Analysis and Implementation of a One-Ground-Diode Three-Switch Active-Clamp Forward Converter

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Abstract

A one-ground-diode three-switch active-clamp forward converter is proposed in this paper. The proposed converter exhibits the features of wide-input voltage-range application and high efficiency. All the switches of the proposed converter can achieve zero-voltage switching (ZVS) under turn-on transition. The operating principle of the proposed converter is presented in detail herein. A 400 V input voltage, 48 V output voltage, 400 W output power prototype of converter is implemented. Based on simulations and experimental results, the theoretical analysis is thus verified. Moreover, it reveals from experimental results that the maximum power efficiency of the proposed converter is 90.1 % at output power of 400 W.

Keywords: active-clamp, forward converter, zero-voltage switching (ZVS).

1. Introduction

For the low-to-medium power applications, a forward converter is widely and often adopted because of its simplicity and high reliability. In the forward converter, the transformer is used to achieve galvanic isolation and high input to output step up or down in voltage. The flux of the magnetizing inductor should thereby be reset during a switching period in a steady-state operation to avoid transformer core saturation (1-10). As a result, the tertiary reset winding (1-2), hybrid-bridge switching circuit (3-4), RCD reset circuit (5-6) and active-clamp reset circuit (7-8) were proposed and applied to the forward converter. However, both the tertiary-winding forward converter and hybrid-bridge forward converter were limited to below a

maximum duty cycle, which is 50 % sometimes, to insure proper reset of the transformer. RCD type forward converters were presented to enable stretching the maximum duty cycles above 50 %, particularly useful in wide range input supply designs. Nevertheless, the power consumption of the resistor in the RCD reset circuit degrades the overall efficiency of the converter. Moreover, the penalty for the high voltage stress on the semiconductors will also be paid with this adaptation.

In order to obtain the higher power density of a dc-dc power converter, the converter may operate at a higher switching frequency. However, the switching losses increase and the efficiency decreases with increasing frequency. To overcome this drawback, the soft switching techniques are taken into consideration (7-10). As a result, a conventional active-clamp forward converter as shown in Fig. 1 is thus presented to obtain zero-voltage switching (ZVS) operation at turn-on transition for all the switches.

Unfortunately, an active-clamp forward converter still exhibits the drawback of the high voltage stress on the main switch. In order to share the high voltage stress of $V_{in} + V_{ce}$, two main switches are thus applied. In practice, the voltage stress cannot be half shared because of the two unmatched main switches. It makes one of the two main switches may suffer from the full voltage stress of $V_{in} + V_{ce}$. Therefore, a one ground diode is utilized to derive the proposed converter herein as depicted in Fig 2. It reveals that the voltage stress of switch S_1 is clamped to V_{ce} , and the voltage stress of switch S_2 is clamped to V_{in} . Notably, as the duty cycle is operated at 0.5, the voltage stresses across the main switches S_1 and S_2 are both equal to the input voltage.

Fig. 1. Conventional active-clamp forward converter.

Fig. 2. Proposed one-ground-diode three-switch active-clamp forward converter.

2. Operating Principle

The proposed one-ground-diode three-switch active-clamp forward converter presented in Fig. 2 contains two main switches S_1 , S_2 , one auxiliary switch S_3 in active-clamp circuit and one ground diode D_c . The proposed converter exhibits the features of wide-input voltage-range application due to the unlimited duty cycle, high efficiency owing to the ZVS operation achieved for all switches and low voltage stress across the main switches S_1 , S_2 .

Some assumptions are made as follows before describing the operating principle of the proposed converter.

- 1) All switches and diodes of the proposed converter are ideal. The switching time of the switches and the reverse recovery time of the diodes can be neglected.
- 2) The time interval of the resonance and the charge and discharge time of capacitors C_{S1} , C_{S2} , C_{S3} are much smaller than switching period T_s , and thus the inductor currents i_{Lm} and i_{Lo} are considered as constants $i_{Lm}^{\max}$ and $i_{Lo}^{\max}$ during the turn-off transition, and $i_{Lm}^{\min}$ and $i_{Lo}^{\min}$ during the turn-on transition, respectively.
- 3) The clamp capacitor C_c and output capacitor C_o are large enough so that their voltages are regarded as constant voltages V_{Cc} and V_o , respectively.

- 4) In the steady state and neglecting the dead time interval, we can derive the following equations based on the voltage-second balance principle to the magnetizing inductor L_m and output inductor L_o .

$$V_{Cc} = \frac{D}{1-D} V_{in} \quad (1)$$

$$\frac{V_o}{V_{in}} = nD \quad (2)$$

Based on the switching of the switches and diodes, the proposed converter operating over one switching period T_s can be divided into eight linear stages described as follows. The equivalent circuit of each stage is presented in Fig. 3.

Stage 1 $[t_0, t_1]$ (S_1 :on, S_2 :on $\rightarrow$ off, S_3 :off, D_c :off, D_1 :off, D_2 :off, D_3 :off, D_{S1} :on, D_{S2} :off)

Before time t_0 , the switches S_1 , S_2 , S_3 are respectively on, on and off. The circuit operation has been achieved steady state. When the switch S_2 is turned on at time t_0 , this stage starts. In this stage, the capacitor C_{S2} are charged linearly by constant current i_1 , and the capacitor C_{S2} is discharged linearly by constant current i_2 . Notably, the currents i_1 and i_2 are satisfied the equality of $i_{Lr} = i_1 + i_2$. The inductor current i_{Lr} and capacitor voltages v_{CS1} , v_{CS2} , v_{CS3} are thus expressed as

$$i_{Lr}(t) = i_{Lm}^{\max} + n i_{Lo}^{\max} \quad (3)$$

$$v_{CS1}(t) = 0 \quad (4)$$

$$v_{CS2}(t) = \frac{i_{Lm}^{\max} + n i_{Lo}^{\max}}{C_{S2} + C_{S3}} (t - t_0) \quad (5)$$

$$v_{CS3}(t) = V_{in} + V_{Cc} - \frac{i_{Lm}^{\max} + n i_{Lo}^{\max}}{C_{S2} + C_{S3}} (t - t_0) \quad (6)$$

When the voltage v_{CS2} increases to V_{in} and voltage v_{CS3} drops to V_{Cc} , the diode D_c thereby conducts and this stage ends.

Stage 2 $[t_1, t_2]$ (S_1 :on, S_2 :off, S_3 :off, D_c : on, D_1 :off, D_2 :off, D_3 :off, D_{S1} :on, D_{S2} :on)

As the diode D_c conducts, the voltages v_{CS2} and v_{CS3} are clamped at V_{in} and V_{Cc} , respectively. In this stage, the inductor current i_{Lr} and capacitor voltages v_{CS1} , v_{CS2} , v_{CS3} are fixed and shown as

$$i_{Lr}(t) = i_{Lm}^{\max} + n i_{Lo}^{\max} \quad (7)$$

$$v_{CS1}(t) = 0 \quad (8)$$

$$v_{C_{S2}}(t) = V_{in} \quad (9)$$

$$v_{C_{S3}}(t) = V_{Cc} \quad (10)$$

In this stage, the transformer primary voltage is also clamped at zero, the currents of the rectifier diodes D_{S1} , D_{S2} are prepared to commute. The stage ends when the main switch S_1 is turned off.

Stage 3 [t_2, t_3] (S_1 :on→off, S_2 :off, S_3 :off, D_c :on, D_1 :off, D_2 :off, D_3 :off, D_{S1} :on, D_{S2} :on)

As the diodes D_{S1} and D_{S2} both conducts, the transformer primary and secondary voltages are thus clamped at zero in this stage. The current is commutated from D_{S1} to D_{S2} , and the resonance between L_r and $(C_{S1} + C_{S3})$ is also occurred. When the voltage $v_{C_{S1}}$ is charged to V_{Cc} , and the voltage $v_{C_{S3}}$ is discharge to zero simultaneously. In the meanwhile, the diode D_3 starts to conduct and the resonance is stopped. In this stage, we have

$$i_{Lr}(t) = (i_{Lm}^{\max} + ni_{Lo}^{\max}) \cos \omega_1(t - t_2) \quad (11)$$

$$v_{C_{S1}}(t) = Z_1(i_{Lm}^{\max} + ni_{Lo}^{\max}) \sin \omega_1(t - t_2) \quad (12)$$

$$v_{S3}(t) = V_{Cc} - Z_1(i_{Lm}^{\max} + ni_{Lo}^{\max}) \sin \omega_1(t - t_2) \quad (13)$$

where $\omega_1 := 1/\sqrt{L_r(C_{S1} + C_{S3})}$ and $Z_1 := \sqrt{L_r/(C_{S1} + C_{S3})}$.

Stage 4 [t_3, t_4] (S_1 :off, S_2 :off, S_3 :off, D_c :off, D_1 :off, D_2 :off, D_3 :on, D_{S1} :on, D_{S2} :on)

As the diode D_3 is forward-biased, the voltage $v_{C_{S3}}$ is clamped at zero. The switch S_3 can be thereby turned on under ZVS operation. Because the voltage across to the inductor L_r is $-V_{Cc}$, the inductor current thus decreases linearly. During this stage, it yields

$$i_{Lr}(t) = -\frac{V_{Cc}}{L_r}(t - t_3) + i_{Lr}(t_3) \quad (14)$$

$$v_{C_{S1}}(t) = V_{Cc} \quad (15)$$

$$v_{C_{S2}}(t) = V_{in} \quad (16)$$

$$v_{C_{S3}}(t) = 0 \quad (17)$$

To ensure the ZVS operation for the switch S_3 , the inductor current i_{Lr} is still negative at the end of this stage. Therefore, it obtains

$$i_{Lr}(t_4) = -\frac{V_{Cc}}{L_r}(t_4 - t_3) + i_{Lr}(t_3) > 0 \quad (18)$$

Stage 5 [t_4, t_5] (S_1 :off, S_2 :off, S_3 :off→on, D_c :off, D_1 :off, D_2 :off, D_3 :on, D_{S1} :on, D_{S2} :on)

In this stage, the circuit operation is the same as that in stage 4. The current i_{Lr} continues to fall linearly until $i_{Lr}(t_5) = i_{Lm}^{\max}$ at time t_5 . At this moment, the current commutation between D_{S1} and D_{S2} is also finished.

Stage 6 [t_5, t_6] (S_1 :off, S_2 :off, S_3 :on, D_c :off, D_1 :off,

D_2 :off, D_3 :on, D_{S1} :on, D_{S2} :off)

After the diode D_{S1} becomes reverse-biased, the transformer primary voltage is not clamped at zero anymore. Therefore, the inductor currents i_{Lr} and i_{Lm} are started to linearly decrease with the same slope of $-V_{Cc}/(L_m + L_r)$. It can obtain

$$i_{Lr}(t) = i_{Lm}^{\max} - V_{Cc}(t - t_5)/(L_m + L_r) \quad (19)$$

In this stage, the circuit operation is the same as the turn-off state of a conventional two-switch forward converter.

Stage 7 [t_6, t_7] (S_1 :off, S_2 :off, S_3 :on→off, D_c :off, D_1 :off, D_2 :off, D_3 :off, D_{S1} :on, D_{S2} :off)

At time t_6 , the switch S_3 is turned off and thus this stage begins. In this stage, the capacitors C_{S1} and C_{S2} are discharged linearly by constant current i_4 , and the capacitor C_{S2} is charged linearly by constant current i_3 . Notably, the currents i_3 and i_4 are satisfied the equality of $i_{Lr} = i_3 + i_4$. The inductor current i_{Lr} and capacitor voltages $v_{C_{S1}}$, $v_{C_{S2}}$, $v_{C_{S3}}$ are thus expressed as

$$i_{Lr}(t_6) = i_{Lm}^{\min} \quad (20)$$

$$v_{C_{S1}}(t) = V_{Cc} + \frac{i_{Lm}^{\min}}{C_S + C_{S3}}(t - t_6) \quad (21)$$

$$v_{C_{S2}}(t) = V_{in} + \frac{i_{Lm}^{\min}}{C_S + C_{S3}}(t - t_6) \quad (22)$$

$$v_{C_{S3}}(t) = -\frac{i_{Lm}^{\min}}{C_S + C_{S3}}(t - t_6) \quad (23)$$

When the voltage $v_{C_{S3}}$ increases to V_{Cc} and voltage $v_{C_{S3}}$ drops to V_{Cc} , the diode D_2 thereby conducts and this stage ends.

Stage 8 [t_6, t_7] (S_1 :off, S_2 :off, S_3 :off, D_c :off, D_1 :off, D_2 :off, D_3 :off, D_{S1} :on, D_{S2} :on)

As the diode D_3 conducts, transformer primary voltage is clamped at zero. It makes the current commutation between D_{S1} and D_{S2} occur. The capacitor voltages $v_{C_{S1}}$ and v_{C_2} continue to decrease owing to the resonance between L_r and $(C_{S1} + C_{S2})$. Therefore, one gets

$$i_{Lr}(t) = i_{Lm}^{\min} \cos \omega_2(t - t_7) \quad (24)$$

$$v_{C_{S1}} = v_{C_{S1}}(t_7) + Z_2 i_{Lm}^{\min} \sin \omega_2(t - t_7) \quad (25)$$

$$v_{C_{S2}} = v_{C_{S2}}(t_7) + Z_2 i_{Lm}^{\min} \sin \omega_2(t - t_7) \quad (26)$$

where $\omega_2 := 1/\sqrt{L_r C_S}$ and $Z_2 := \sqrt{L_r/C_S}$.

As the voltage $v_{C_{S1}}$ falls to zero, the diode D_1 becomes forward-biased and this stage ends.

(a) Stage 1 : $[t_0, t_1]$

(b) Stage 2 : $[t_1, t_2]$

(c) Stage 3 : $[t_2, t_3]$

(d) Stage 4 : $[t_3, t_4]$

(e) Stage 5 : $[t_4, t_5]$

(f) Stage 6 : $[t_5, t_6]$

(g) Stage 7 : $[t_6, t_7]$

(h) Stage 8 : $[t_7, t_8]$

(i) Stage 9 : $[t_8, t_9]$

(j) Stage 10 : $[t_9, t_{10}]$

(k) Stage 11 : $[t_{10}, t_{11}]$

(l) Stage 12 : $[t_{11}, t_0 + T_s]$

Fig. 3. Equivalent circuit of each linear stage.

Stage 9 [t_8, t_9] (S_1 :off, S_2 :off, S_3 :off, D_c :off, D_1 :on, D_2 :off, D_3 :off, D_{S1} :on, D_{S2} :on)

Because the diode D_1 conducts, the voltage v_{CS1} is clamped at zero. The main switch S_1 can be thereby turned on under ZVS operation. Moreover, the resonance between L_r and C_{S2} is still operated to cause the capacitor voltage v_{C2} decrease to zero. The diode D_2 is thus conducted, and this stage is finished. Similarly, the main switch S_2 can also be turned on under ZVS operation at the next stage. In this stage, we have

$$i_{Lr}(t) = i_{Lr}(t_8) \cos \omega_3(t - t_8) \quad (27)$$

$$v_{CS2}(t) = v_{CS1}(t_8) + Z_3 i_{Lr}(t_8) \sin \omega_3(t - t_8) \quad (28)$$

where $\omega_3 := 1/\sqrt{L_r C_{S2}}$ and $Z_3 := \sqrt{L_r/C_{S2}}$.

Stage 10 [t_9, t_{10}] (S_1 :off, S_2 :off, S_3 :off, D_c :off, D_1 :on, D_2 :on, D_3 :off, D_{S1} :on, D_{S2} :on)

In this stage, the inductor currents i_{Lr} is started to linearly increase with the slope of V_{in}/L_r . Then it gives

$$i_{Lr}(t) = i_{Lr}(t_9) + V_{in}(t - t_9)/L_r \quad (29)$$

Both the switches S_1 and S_2 are turned on under ZVS condition at time t_{10} . Notably, it reveals that the ZVS operation for switches S_1 and S_2 can be achieved if the following inequality equation should be satisfied.

$$i_{Lr}(t_{10}) < 0 \quad (30)$$

Stage 11 [t_{10}, t_{11}] (S_1 :on, S_2 :on, S_3 :off, D_c :off, D_1 :off, D_2 :off, D_3 :off, D_{S1} :on, D_{S2} :on)

In this stage, the circuit operation is the same as that in stage 10. The current i_{Lr} continues to rise linearly until $i_{Lr}(t_{11}) = i_{Lm}^{\min} + N_1 i_{Lo}^{\min}/N_2$ at time t_{11} . The current commutation between D_{S1} and D_{S2} is thus finished.

Stage 12 [$t_{11}, t_0 + T_s$] (S_1 : on, S_2 : on, S_3 :off, D_c :off, D_1 :off, D_2 :off, D_3 :off, D_{S1} :off, D_{S2} :on)

After the diode D_{S1} becomes reverse-biased, the inductor currents i_{Lr} and i_{Lm} are started to linearly increase with the same slope of $V_{in}/(L_m + L_r)$. Simultaneously, the output inductor current i_{Lo} is increased linearly from $i_{Lo}^{\min}$ with the slope of $N_2 V_{in}/(N_1 L_o)$. In this stage, the circuit operation is the same as the turn-on state of a conventional two-switch forward converter.

The next switching period starts when S_2 is turned on again. According to the aforementioned operating principle of the proposed converter, the key waveforms

over one switching period T_s are schematically depicted in Fig. 4.

Fig.4. Key waveforms over one switching period T_s .

3. Simulations and Experimental Results

For 400 V input and 48 V 400 W output, a prototype of the proposed one-ground-diode three-switch active-clamp forward converter, operating at 100 kHz, is implemented. Based on the simulations and experimental results, the soft-switching performance of all the switches and the high power efficiency of the proposed converter can thus be validated. The power specifications and component parameters are listed in Table 1.

Table 1. Power specifications and component parameters.

V_{in}	400 V	P_o	100 ~ 400 W
V_o	48 V	f_s	100 kHz
N_2/N_1	0.26	L	300 μ H
L_m	316 μ H	L_r	74 μ H
C_C	0.22 μ F	C_o	100 μ F
C_{S1}, C_{S2}	350 pF	C_{S3}	380 pF
S_1, S_2	STP20NM60	S_3	W7NA90

3.1 Steady-state characteristic

It reveals from Fig. 7 that the input voltage V_{in} is 400 V and the output voltage V_o is 48 V. Moreover, according to the gating signal v_{gs1} in Fig. 5, we have the duty ratio

$D = 0.46$ and $D = 0.48$ from simulation and experimental results, respectively. Both of them are close to the duty ratio $D = 0.46$ derived from Eq. (1) in the theoretical analysis.

3.2 Soft-switching performance

Figs. 6-8 show the simulations and experimental results of drain-to-source voltages and gating signals of all the switches. It reveals that the switches are turned on after their drain-to-source voltages drop to zero. As a result, all the switches of the proposed converter are achieved ZVS operation at turn-on transition. Moreover, we also can find that the maximum voltages across switches S_1 and S_2 are nearly input voltage $V_{in} = 400\text{ V}$.

3.3 Power efficiency measurement

Fig. 9 shows the measured efficiency versus various output power. The efficiency at different load conditions is also listed in the Table 2. The highest efficiency of the proposed converter is about 90.1 %. The efficiency of the proposed converter can be further improved by using synchronous rectification.

Fig. 5. Waveforms of gating signal v_{gs1} , input voltage V_{in} and output voltage V_o at full load.

Fig. 6. Waveforms of gating signal and drain-to-source voltage of switch S_1 at full load.

Fig. 7. Waveforms of gating signal and drain-to-source voltage of switch S_2 at full load.

Fig. 8. Waveforms of gating signal and drain-to-source voltage of switch S_3 at full load.

Fig. 9. Measured efficiency versus various output power.

Table 2. Measured efficiency at various output power.

Output power (W)	100	150	200	250	300	350	400
Efficiency(%)	86.1	89.0	90.4	91.1	91.4	91.4	91.0

4. Conclusions

A one-ground-diode three-switch active-clamp forward converter is proposed to achieve ZVS operation under turn-on transition for all switches. It can be used for wide-range input voltage and high efficiency applications.

The voltage stress across the two main switches can be approximately to the input voltage V_{in} as the operated duty cycle $D \approx 0.5$. The simulations and experimental results of a prototype with 400V input and 48 V/400 W output verify the theoretical analysis and performance of the proposed converter. The measured maximum power efficiency of the proposed converter is 90 % at output power of 400 W.

Acknowledgment

The authors would like to thank the Ministry of Science and Technology, Taiwan, for supporting this research under Contract No. MOST 103-2221-E-168-011.

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