Analysis and Implementation of a One-Ground-Diode Three-Switch Active-Clamp Forward Converter

*Sung-Pei Yang, Shin-Ju Chen, Chao-Ming Huang and Chieh-Lung Shih

Department of Electrical Engineering, Kun Shan University,
No.195, Kunda Rd., Tainan City 710, Taiwan, R.O.C.

*Corresponding Author: spyang@mail.ksu.edu.tw

Abstract

A one-ground-diode three-switch active-clamp forward converter is proposed in this paper. The proposed converter exhibits the features of wide-input voltage-range application and high efficiency. All the switches of the proposed converter can achieve zero-voltage switching (ZVS) under turn-on transition. The operating principle of the proposed converter is presented in detail herein. A 400 V input voltage, 48 V output voltage, 400 W output power prototype of converter is implemented. Based on simulations and experimental results, the theoretical analysis is thus verified. Moreover, it reveals from experimental results that the maximum power efficiency of the proposed converter is 90.1 % at output power of 400 W.

Keywords: active-clamp, forward converter, zero-voltage switching (ZVS).

1. Introduction

For the low-to-medium power applications, a forward converter is widely and often adopted because of its simplicity and high reliability. In the forward converter, the transformer is used to achieve galvanic isolation and high input to output step up or down in voltage. The flux of the magnetizing inductor should thereby be reset during a switching period in a steady-state operation to avoid transformer core saturation (1-10). As a result, the tertiary reset winding (1-2), hybrid-bridge switching circuit (3-4), RCD reset circuit (5-6) and active-clamp reset circuit (7-8) were proposed and applied to the forward converter. However, both the tertiary-winding forward converter and hybrid-bridge forward converter were limited to below a maximum duty cycle, which is 50 % sometimes, to insure proper reset of the transformer. RCD type forward converters were presented to enable stretching the maximum duty cycles above 50 %, particularly useful in wide range input supply designs. Nevertheless, the power consumption of the resistor in the RCD reset circuit degrades the overall efficiency of the converter. Moreover, the penalty for the high voltage stress on the semiconductors will also be paid with this adaptation.

In order to obtain the higher power density of a dc-dc power converter, the converter may operate at a higher switching frequency. However, the switching losses increase and the efficiency decreases with increasing frequency. To overcome this drawback, the soft switching techniques are taken into consideration (7-10). As a result, a conventional active-clamp forward converter as shown in Fig. 1 is thus presented to obtain zero-voltage switching (ZVS) operation at turn-on transition for all the switches.

Unfortunately, an active-clamp forward converter still exhibits the drawback of the high voltage stress on the main switch. In order to share the high voltage stress of $V_n + V_c$ , two main switches are thus applied. In practice, the voltage stress cannot be half shared because of the two unmatched main switches. It makes one of the two main switches may suffer from the full voltage stress of $V_n + V_c$. Therefore, a one ground diode is utilized to derive the proposed converter herein as depicted in Fig 2. It reveals that the voltage stress of switch $S_1$ is clamped to $V_c$, and the voltage stress of switch $S_2$ is clamped to $V_n$. Notably, as the duty cycle is operated at 0.5, the voltage stresses across the main switches $S_1$ and $S_2$ are both equal to the input voltage.
The inductor current active-clamp circuit and one ground diode switches and low voltage stress across the main switches voltage-range application due to the unlimited duty cycle, proposed converter exhibits the features of wide-input two main switches 1 active-clamp forward converter presented in Fig. 2 contains clamp forward converter.

The proposed one-ground-diode three-switch active-clamp forward converter presented in Fig. 2 contains two main switches $S_1$, $S_2$, one auxiliary switch $S_3$ in active-clamp circuit and one ground diode $D_3$. The proposed converter exhibits the features of wide-input voltage-range application due to the unlimited duty cycle, high efficiency owing to the ZVS operation achieved for all switches and low voltage stress across the main switches $S_1$, $S_2$.

Some assumptions are made as follows before describing the operating principle of the proposed converter.

1) All switches and diodes of the proposed converter are ideal. The switching time of the switches and the reverse recovery time of the diodes can be neglected.

2) The time interval of the resonance and the charge and discharge time of capacitors $C_{s1}$, $C_{s2}$, $C_{s3}$ are much smaller than switching period $T_s$, and thus the inductor currents $i_{Lm}$ and $i_{Lo}$ are considered as constants $i_{Lm}^{max}$ and $i_{Lo}^{max}$ during the turn-off transition, and $i_{Lm}^{min}$ and $i_{Lo}^{min}$ during the turn-on transition, respectively.

3) The clamp capacitor $C_c$ and output capacitor $C_o$ are large enough so that their voltages are regarded as constant voltages $V_{c}$ and $V_o$, respectively.

4) In the steady state and neglecting the dead time interval, we can derive the following equations based on the voltage-second balance principle to the magnetizing inductor $L_m$ and output inductor $L_o$.

$$ V_C = \frac{D}{1-D}V_{in} $$

$$ \frac{V_o}{V_{in}} = nD $$

Based on the switching of the switches and diodes, the proposed converter operating over one switching period $T_s$ can be divided into eight linear stages described as follows. The equivalent circuit of each stage is presented in Fig. 3.

**Stage 1** $[t_0, t_1]$ ($S_1$:on, $S_2$:on→off, $S_3$:off, $D_1$:off, $D_2$:off, $D_3$:off, $D_4$:on, $D_5$:off)

Before time $t_0$, the switches $S_1$, $S_2$, $S_3$ are respectively on, on and off. The circuit operation has been achieved steady state. When the switch $S_2$ is turned on at time $t_0$, this stage starts. In this stage, the capacitor $C_{s2}$ are charged linearly by constant current $i_1$, and the capacitor $C_{s3}$ is discharged linearly by constant current $i_2$. Notably, the currents $i_1$ and $i_2$ are satisfied the equality of $i_{Lr} = i_1 + i_2$. The inductor current $i_{Lr}$ and capacitor voltages $v_{c31}$, $v_{c32}$, $v_{c33}$ are thus expressed as

$$ i_{Lr}(t) = i_{Lr}^{max} + n_1^{max}i_{Lm} $$

$$ v_{c31}(t) = 0 $$

$$ v_{c32}(t) = i_{Lr}^{max} + n_2^{max}i_{Lm} - \frac{C_{s3}}{C_{s2} + C_{s3}}(t-t_0) $$

$$ v_{c33}(t) = V_o + V_{c} - \frac{i_{Lr}^{max} + n_3^{max}i_{Lm}}{C_{s3}}(t-t_0) $$

When the voltage $v_{c32}$ increases to $V_o$ and voltage $v_{c33}$ drops to $V_{c}$, the diode $D_4$ thereby conducts and this stage ends.

**Stage 2** $[t_1, t_2]$ ($S_1$:on, $S_2$:off, $S_3$:off, $D_1$:on, $D_2$:off, $D_3$:off, $D_4$:on, $D_5$:on)

As the diode $D_4$ conducts, the voltages $v_{c32}$ and $v_{c33}$ are clamped at $V_o$ and $V_{c}$, respectively. In this stage, the inductor current $i_{Lr}$ and capacitor voltages $v_{c31}$, $v_{c32}$, $v_{c33}$ are fixed and shown as

$$ i_{Lr}(t) = i_{Lr}^{max} + n_1^{max}i_{Lm} $$

$$ v_{c31}(t) = 0 $$
\[ v_{c2}(t) = V_w. \quad (9) \]
\[ v_{c2}(t) = V_c. \quad (10) \]

In this stage, the transformer primary voltage is also clamped at zero, the currents of the rectifier diodes \( D_{S1}, D_{S2} \) are prepared to commutate. The stage ends when the main switch \( S_3 \) is turned off.

**Stage 3 \([t_5, t_6]\) \((S_1: on->off, S_2: off, S_3: off, D_2: off, D_3: off, D_5: on, D_6: on)\)**

As the diodes \( D_{S1} \) and \( D_{S2} \) both conducts, the transformer primary and secondary voltages are thus clamped at zero in this stage. The current is commutated from \( D_{S1} \) to \( D_{S2} \), and the current is decreased. The stage ends when the voltage \( v_{c31} \) is clamped to \( V_c \), and the voltage \( v_{c32} \) is discharge to zero simultaneously. In the meanwhile, the diode \( D_{S1} \) starts to conduct and the resonance is stopped. In this stage, we have

\[ i_{r_1}(t) = (i_{sw1}^{max} + n i_{sw1}^{min}) \cos \omega_1 (t - t_5) \quad (11) \]
\[ v_{c31}(t) = Z_i (i_{sw1}^{max} + n i_{sw1}^{min}) \sin \omega_1 (t - t_5) \quad (12) \]
\[ v_{c32}(t) = V_c - Z_i (i_{sw1}^{max} + n i_{sw1}^{min}) \sin \omega_1 (t - t_5) \quad (13) \]

where \( \omega_1 = 1/\sqrt{L_i (C_{S1} + C_{S2})} \) and \( Z_i = \sqrt{L_i / (C_{S1} + C_{S2})} \).

**Stage 4 \([t_5, t_6]\) \((S_1: off, S_2: off, S_3: off, D_2: off, D_3: off, D_5: on, D_6: on)\)**

As the diode \( D_1 \) is forward-biased, the voltage \( v_{c31} \) is clamped at zero. The switch \( S_1 \) can be thereby turned on under ZVS operation. Because the voltage across to the inductor \( L_r \) is \(-V_c\), the inductor current thus decreases linearly. During this stage, it yields

\[ i_{r_1}(t) = \frac{V_c}{L_r} (t - t_5) + i_{r_1}(t_5) \quad (14) \]
\[ v_{c31}(t) = V_c \quad (15) \]
\[ v_{c32}(t) = V_w \quad (16) \]
\[ i_{r_1}(t) = 0 \quad (17) \]

To ensure the ZVS operation for the switch \( S_1 \), the inductor current \( i_{r_1} \) is still negative at the end of this stage. Therefore, it obtains

\[ i_{r_1}(t) = \frac{V_c}{L_r} (t - t_5) + i_{r_1}(t_5) > 0 \quad (18) \]

**Stage 5 \([t_5, t_6]\) \((S_1: off, S_2: off, S_3: off->on, D_2: off, D_3: off, D_5: on, D_6: on)\)**

In this stage, the circuit operation is the same as that in stage 4. The current \( i_{r_1} \) continues to fall linearly until \( i_{r_1}(t_6) = i_{sw1}^{max} \) at time \( t_6 \). At this moment, the current commutation between \( D_{S1} \) and \( D_{S2} \) is also finished.

**Stage 6 \([t_5, t_6]\) \((S_1: off, S_2: off, S_3: on, D_2: off, D_3: off, D_5: off, D_6: on)\)**

After the diode \( D_{S1} \) becomes reverse-biased, the transformer primary voltage is not clamped at zero anymore. Therefore, the inductor currents \( i_{r_1} \) and \( i_{r_2} \) are started to linearly decrease with the same slope of \(-V_c / (L_r + L_r)\). It can obtain

\[ i_{r_1}(t) = i_{sw1}^{max} - V_c (t - t_5) / (L_r + L_r) \quad (19) \]

where \( \omega_2 = 1/\sqrt{L_r C_S} \) and \( Z_2 = \sqrt{L_r / C_S} \).

As the voltage \( v_{c31} \) falls to zero, the diode \( D_1 \) becomes forward-biased and this stage ends.
Fig. 3. Equivalent circuit of each linear stage.

Because the diode \(D_1\) conducts, the voltage \(v_{c31}\) is clamped at zero. The main switch \(S_i\) can be thereby turned on under ZVS operation. Moreover, the resonance between \(L_r\) and \(C_{s2}\) is still operated to cause the capacitor voltage \(v_{c2}\) decrease to zero. The diode \(D_2\) is thus conducted, and this stage is finished. Similarly, the main switch \(S_j\) can also be turned on under ZVS operation at the next stage. In this stage, we have

\[
i_{L_r}(t) = i_{L_r}(t_9) \cos \omega_r (t - t_9)
\]

\[
v_{c22}(t) = v_{c31}(t_9) + Z_i i_{L_r}(t_9) \sin \omega_r (t - t_9)
\]

where \(\omega_r := 1/\sqrt{L_r C_{s2}}\) and \(Z_i := \sqrt{L_r/C_{s2}}\).

Stage 10 \([t_0, t_{10}] \) \((S_{1:off}, S_{2:off}, S_{3:off}, D_{1:off}, D_{2:off}, D_{3:off}, D_{4:off}, D_{5:off}, D_{6:off}, D_{7:off}, D_{8:off}, D_{9:off}, D_{10:off})\)

In this stage, the inductor currents \(i_{L_r}\) is started to linearly increase with the slope of \(V_a/L_r\). Then it gives

\[
i_{L_r}(t) = i_{L_r}(t_9) + V_a(t - t_9)/L_r
\]

Both the switches \(S_i\) and \(S_j\) are turned on under ZVS condition at time \(t_{10}\). Notably, it reveals that the ZVS operation for switches \(S_i\) and \(S_j\) can be achieved if the following inequality equation should be satisfied.

\[
i_{L_r}(t_9) < 0
\]

Stage 11 \([t_{10}, t_{11}] \) \((S_{1:on}, S_{2:on}, S_{3:off}, D_{1:off}, D_{2:off}, D_{3:off}, D_{4:off}, D_{5:off}, D_{6:off}, D_{7:off}, D_{8:off}, D_{9:off}, D_{10:off})\)

In this stage, the circuit operation is the same as that in stage 10. The current \(i_{L_r}\) continues to rise linearly until \(i_{L_r}(t_{11}) = i_{L_r}^{\max} + N_j i_{L_r}^{\max}/N_i\) at time \(t_{11}\). The current commutation between \(D_{31}\) and \(D_{21}\) is thus finished.

Stage 12 \([t_{11}, t_0 + T_s]\) \((S_{1:on}, S_{2:on}, S_{3:off}, D_{1:off}, D_{2:off}, D_{3:off}, D_{4:off}, D_{5:off}, D_{6:off}, D_{7:off}, D_{8:off}, D_{9:off}, D_{10:off})\)

After the diode \(D_{31}\) becomes reverse-biased, the inductor currents \(i_{L_r}\) and \(i_{L_m}\) are started to linearly increase with the same slope of \(V_a/(L_m + L_r)\). Simultaneously, the output inductor current \(i_{L_m}\) is increased linearly from \(i_{L_m}^{\max}\) with the slope of \(N_j V_a/(N_i L_r)\). In this stage, the circuit operation is the same as the turn-on state of a conventional two-switch forward converter.

The next switching period starts when \(S_2\) is turned on again. According to the aforementioned operating principle of the proposed converter, the key waveforms over one switching period \(T_s\) are schematically depicted in Fig. 4.

![Key waveforms over one switching period](image)

### 3. Simulations and Experimental Results

For 400 V input and 48 V 400 W output, a prototype of the proposed one-ground-diode three-switch active-clamp forward converter, operating at 100 kHz, is implemented. Based on the simulations and experimental results, the soft-switching performance of all the switches and the high power efficiency of the proposed converter can thus be validated. The power specifications and component parameters are listed in Table 1.

<table>
<thead>
<tr>
<th>(V_a)</th>
<th>(400) V</th>
<th>(P_o)</th>
<th>(100 \sim 400) W</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_o)</td>
<td>48 V</td>
<td>(f_s)</td>
<td>100 kHz</td>
</tr>
<tr>
<td>(N_s / N_i)</td>
<td>0.26</td>
<td>(L)</td>
<td>300 (\mu)H</td>
</tr>
<tr>
<td>(L_m)</td>
<td>316 (\mu)H</td>
<td>(L_r)</td>
<td>74 (\mu)H</td>
</tr>
<tr>
<td>(C_{C})</td>
<td>0.22 (\mu)F</td>
<td>(C_0)</td>
<td>100 (\mu)F</td>
</tr>
<tr>
<td>(C_{s1}, C_{s2})</td>
<td>350 pF</td>
<td>(C_{s3})</td>
<td>380 pF</td>
</tr>
<tr>
<td>(S_{1}, S_{2})</td>
<td>STP20NM60</td>
<td>(S_{3})</td>
<td>W7NA90</td>
</tr>
</tbody>
</table>

#### 3.1 Steady-state characteristic

It reveals from Fig. 7 that the input voltage \(V_a\) is 400 V and the output voltage \(V_o\) is 48 V. Moreover, according to the gating signal \(v_{g1}\) in Fig. 5, we have the duty ratio
$D = 0.46$ and $D = 0.48$ from simulation and experimental results, respectively. Both of them are close to the duty ratio $D = 0.46$ derived from Eq. (1) in the theoretical analysis.

3.2 Soft-switching performance

Figs. 6-8 show the simulations and experimental results of drain-to-source voltages and gating signals of all the switches. It reveals that the switches are turned on after their drain-to-source voltages drop to zero. As a result, all the switches of the proposed converter are achieved ZVS operation at turn-on transition. Moreover, we also can find that the maximum voltages across switches $S_1$ and $S_2$ are nearly input voltage $V_{in} = 400\, \text{V}$.

3.3 Power efficiency measurement

Fig. 9 shows the measured efficiency versus various output power. The efficiency at different load conditions is also listed in the Table 2. The highest efficiency of the proposed converter is about 90.1 %. The efficiency of the proposed converter can be further improved by using synchronous rectification.
4. Conclusions

A one-ground-diode three-switch active-clamp forward converter is proposed to achieve ZVS operation under turn-on transition for all switches. It can be used for wide-range input voltage and high efficiency applications. The voltage stress across the two main switches can be approximately to the input voltage $V_i$ as the operated duty cycle $D \approx 0.5$. The simulations and experimental results of a prototype with 400V input and 48 V/400 W output verify the theoretical analysis and performance of the proposed converter. The measured maximum power efficiency of the proposed converter is 90 % at output power of 400 W.

Acknowledgment

The authors would like to thank the Ministry of Science and Technology, Taiwan, for supporting this research under Contract No. MOST 103-2221-E-168-011.

References