Analysis and Implementation of a Novel Asymmetrical Half-Bridge High Step-Down DC-DC Converter

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Abstract

A novel asymmetrical half-bridge high step-down (AHB-HSD) dc-dc converter is proposed in this paper. A buck inductor is applied to the conventional asymmetrical half-bridge step-down (AHB-SD) dc-dc converter to achieve the high step-down voltage conversion. Moreover, all switches of the proposed converter can achieve zero-voltage switching (ZVS) under turn-on transition. The operating principle of the proposed converter is presented in detail herein to prove the aforementioned results. Finally, a 400 V input voltage, 48 V output voltage, 400 W output power prototype of proposed converter is implemented. The theoretical analysis is thus verified by experimental results. The maximum power efficiency of the proposed converter is 89.8 % at output power of 250 W.

Keywords: asymmetrical half-bridge (AHB), high step-down (HSD), zero-voltage switching (ZVS).

1. Introduction

A power supply for telecom equipments and modern computers is required to have the characteristic of high power density, which can be achieved by operating at a higher switching frequency. It is well known that the switching losses increase and the efficiency decreases with increasing switching frequency. To overcome this drawback, the soft switching techniques are taken into consideration (1-7). As a result, a conventional asymmetrical half-bridge step-down (AHB-SD) dc-dc converter as shown in Fig. 1 is usually used to obtain zero-voltage switching (ZVS) operation at turn-on transition and low voltage stress for all the switches (5-7). Its output voltage can be determined by

the conversion ratio $V_o/V_{in} = D(1-D)/n$. However, for increasing the step-down conversion ratio with high output current rating applications, one is to get extremely narrow duty cycle, the other is to have a higher turns ratio n of the transformer. Unfortunately, an extremely narrow duty cycle is difficultly controlled to regulate the output voltage. Moreover, the noise is easily affected the narrow duty cycle to cause the converter out of order. To avoid the narrow duty cycle in the high step-down conversion, a higher turns ratio n is thus applied to the transformer of the conventional AHB-SD converter. However, the higher turns ratio will increase the inter-winding capacitances, winding resistances and leakage inductances. It thereby complicates the design and implementation of the transformer. The volume of transformer also becomes large and decreases the power density of the converter.

To solve this problem, many high step-down techniques are thus presented in the literature (8-11). Consequently, a novel asymmetrical half-bridge high step-down (AHB-HSD) dc-dc converter depicted in Fig 2 is proposed by applying a buck inductor L_b to connect with the rectifier diode D_1 . The proposed converter exhibits significant advantages of high step-down conversion ratio, ZVS operation and low voltage stress for all switches, no extremely narrow duty cycle and low turns ratio n of transformer.

Fig. 1. Conventional AHB-SD converter.

Fig. 2. Proposed AHB-HSD converter.

2. Operating Principle

The proposed asymmetrical half-bridge high step-down (AHB-HSD) converter presented in Fig. 2 contains two main switches S_1 , S_2 , which are driven complementarily with two small dead bands to realize the ZVS at turn-on operation for each main switch.

Some assumptions are made as follows before describing the operating principle of the proposed AHB-HSD converter.

- 1) All switches and diodes of the proposed converter are ideal. The switching time of the switches and the reverse recovery time of the diodes can be neglected.
- 2) Because the time intervals of the resonance, the charge and discharge time of capacitors C_{S1} and C_{S2} are much smaller than switching period T_s , the inductor current i_{L_o} are considered as constants $i_{L_o}^{\max}$ during the turn-off transition for switch S_1 , and $i_{L_o}^{\min}$ during the turn-on transition for switch S_1 , respectively.
- 3) The block capacitance C_B and output capacitance C_o are large enough so that their voltages are regarded as constant voltages V_{CB} and V_o , respectively.

- 4) The equivalent inductance is

$$L_e = L_m // (L_b + L_o) = \frac{L_m(L_b + L_o)}{L_m + L_b + L_o} \quad (1)$$

where $L_r \ll L_e$, $L_e < L_m$ and $L_e < L_b + L_o$.

- 5) The turns ratio n of the transformer is 1.

Based on the switching of the switches and diodes, the proposed converter operating over one switching period T_s can be divided into ten linear stages described as follows. The equivalent circuit of each stage is presented in Fig. 3.

Stage 1 [t_0, t_1] (S_1 : off, S_2 : off, D_{S1} : off, D_{S2} : off, D_1 : on, D_2 : off)

Before time t_0 , the switches S_1 and S_2 are on and off, respectively. The circuit operation has been achieved steady state. When the switch S_1 is turned off at time t_0 , this stage starts. In this stage, the capacitor C_{S1} are charged linearly by constant current $i_1(t_0)$, and the capacitor C_{S2} is discharged linearly by constant current $i_2(t_0)$. Notably, the currents i_1 and i_2 are satisfied the equality of $i_{L_r} = i_1 + i_2$. When the voltage v_{ds1} increases to $V_{in} - V_{CB} + L_b V_o / L_o$ and voltage v_{ds2} drops to $V_{CB} - L_b V_o / L_o$, the diode D_2 thereby conducts and this stage ends.

Stage 2 [t_1, t_2] (S_1 : off, S_2 : off, D_{S1} : off, D_{S2} : off, D_1 : on, D_2 : on)

As the diode D_2 conducts, the resonance between $(L_r + L_b // L_m)$ and $(C_{S1} + C_{S2})$ is occurred. When the voltage v_{ds1} is charged to V_{in} , and the voltage v_{ds2} is discharge to zero simultaneously. In the meanwhile, the diode D_{S2} starts to conduct and the resonance is stopped. This stage is thus finished.

Stage 3 [t_2, t_3] (S_1 : off, S_2 : off, D_{S1} : off, D_{S2} : on, D_1 : on, D_2 : on)

As the diode D_{S2} is forward-biased, the voltage v_{ds2} is clamped at zero. The switch S_2 can be thereby turned on under ZVS operation. Because the voltage across to the equivalent inductor $(L_r + L_b // L_m)$ is $-V_{CB}$, the inductor currents i_{L_r} , i_{L_m} and i_{L_b} thus decreases linearly. As the inductor current i_{L_b} falls to zero, the diode D_1 becomes reverse-biased and this stage ends. To ensure the ZVS operation for the switch S_2 , the inductor current i_{L_r} is still positive at the end of this stage.

Stage 4 [t_3, t_4] (S_1 : off, S_2 : on, D_{S1} : off, D_{S2} : on, D_1 : off, D_2 : on)

Since the D_1 is off, the voltage $-V_{CB}$ is thus across to the inductors L_m and L_r . Therefore, the inductor currents i_{L_r} and i_{L_m} still linearly decrease. As the inductor current i_{L_r} falls to zero, the diode D_{S2} becomes off and this stage ends.

Stage 5 [t_4, t_5] (S_1 : off, S_2 : on, D_{S1} : off, D_{S2} : off, D_1 : off, D_2 : on)

In this stage, the circuit operation is similar to the S_1 turn-off state of a conventional AHB-SD converter.

(a) Stage 1 : $[t_0, t_1]$

(b) Stage 2 : $[t_1, t_2]$

(c) Stage 3 : $[t_2, t_3]$

(d) Stage 4 : $[t_3, t_4]$

(e) Stage 5 : $[t_4, t_5]$

(f) Stage 6 : $[t_5, t_6]$

(g) Stage 7 : $[t_6, t_7]$

(h) Stage 8 : $[t_7, t_8]$

(i) Stage 9 : $[t_8, t_9]$

(j) Stage 10 : $[t_9, t_0 + T_s]$

Fig. 3. Equivalent circuit of each linear stage.

Stage 6 $[t_5, t_6]$ (S_1 : off, S_2 : off, D_{S1} : off, D_{S2} : off, D_1 : off, D_2 : on)

At time t_5 , the switch S_2 is turned off and thus this stage begins. In this stage, the capacitor C_{S1} are discharged linearly by constant current $-i_1(t_5)$, and the capacitor C_{S2} is discharged linearly by constant current $-i_2(t_5)$. When the voltage v_{ds1} decreases to $V_{in} - V_{CB}$ and voltage v_{ds2} rises to V_{CB} , the diode D_1 thereby conducts and this stage ends.

Stage 7 $[t_6, t_7]$ (S_1 : off, S_2 : off, D_{S1} : off, D_{S2} : off, D_1 : on, D_2 : on)

As the diode D_1 conducts, the resonance between $(L_r + L_b // L_m)$ and $(C_{S1} + C_{S2})$ is occurred. The inductor current i_{Lb} thus rises by the resonance from zero. When the voltage v_{ds1} is discharged to zero, and the voltage v_{ds2} is charge to V_{in} simultaneously. In the meanwhile, the diode D_{S1} starts to conduct and the resonance is stopped. This stage is thus finished.

Stage 8 $[t_6, t_7]$ (S_1 : off, S_2 : off, D_{S1} : on, D_{S2} : off, D_1 : on, D_2 : on)

As the diode D_{S1} conducts, the voltage v_{CS1} is clamped at zero. The switch S_1 can be thereby turned on under ZVS operation. Because the voltage across to the equivalent inductor $(L_r + L_b // L_m)$ is $V_{in} - V_{CB}$, the inductor currents i_{Lr} , i_{Lm} and i_{Lb} thus increases linearly. As the inductor current i_{Lr} rises to zero, the diode D_{S1} thus becomes off and this stage ends. To ensure the ZVS operation for the switch S_1 , the switch S_1 must turn on before the inductor current i_{Lr} becomes positive.

Stage 9 $[t_8, t_9]$ (S_1 : on, S_2 : off, D_{S1} : off, D_{S2} : off, D_1 : on, D_2 : on)

In this stage, the inductor currents i_{Lr} , i_{Lm} and i_{Lb} still rise linearly. As the inductor current i_{Lb} rises to i_{Lo}^{min} , the diode D_2 thus conducts and this stage ends.

Stage 10 $[t_9, t_0 + T_s]$ (S_1 : on, S_2 : off, D_{S1} : off, D_{S2} : off, D_1 : on, D_2 : on)

In this stage, the circuit operation is similar to the S_1 turn-on state of a conventional AHB-SD converter.

The next switching period starts when S_1 is turned off again. According to the aforementioned operating principle of the proposed converter, the key waveforms over one switching period T_s are schematically depicted in Fig. 4.

Fig.4. Key waveforms over one switching period T_s .

Neglecting the dead times for brief steady-state analysis, the duty cycles of main switches S_1 and S_2 will thus be D and $1 - D$, respectively. In the steady state, based on the voltage-second balance principle to the magnetizing inductor L_m , it shows that voltage V_{CB} is a function as

$$V_{CB} = g(V_{in}, D, k, R) \quad (2)$$

where $k = T_9 / T_s$. Moreover, at the end of the stage 9, the inductor current i_{La} must reach the current i_{Lo}^{min} . It gives

$$\frac{V_{in} - V_{CB}}{L_b + L_r} T_9 = \frac{V_o}{R} - \frac{1}{2} \frac{V_o}{L_o} ((1-D)T_s + T_9). \quad (3)$$

Similarly, according to the voltage-second balance principle to the output inductor L_o , we thus have

$$\frac{V_o}{L_o} ((1-D)T_s + T_9) = \frac{1}{L_b + L_o} (V_{in} - V_{CB} - V_o) (DT_s - T_9). \quad (4)$$

Solving equations (3) and (4), thus it yields

$$V_o = f(V_{in}, D, k, R) \quad (5)$$

where $f(V_{in}, D, k, R)$ is a function of variables V_{in} , D , k and R .

3. Experimental Results

For 400 V input and 48 V 400 W output, a prototype of the proposed AHB-HSD converter, operating at 100 kHz, is implemented. Based on the experimental results, the

soft-switching performance of all the switches and the high power efficiency of the proposed converter can thus be validated. The power specifications and component parameters are listed in Table 1.

Table 1. Power specifications and component parameters.

V_{in}	400 V	V_o	48 V
P_o	100 ~ 400 W	f_s	100 kHz
n	1	L_m	302 μ H
L_b	4 μ H	L_o	207 μ H
C_B	33 μ F	L_r	25 μ H
C_{S1}, C_{S2}	1250 pF	C_o	1000 μ F

3.1 Steady-state characteristic

It reveals from Fig. 5 that the input voltage V_{in} is 400 V and the output voltage V_o is 48 V at full load. Moreover, according to the gating signal v_{gs1} of the experimental result in Fig. 5, we have the duty cycle $D = 0.46$, which is not a narrow duty cycle. However, for the conventional AHB-SD converter, its output voltage V_o is 99.3 V with $D = 0.46$ and $n = 1$, which is much larger than 48 V.

Fig. 5. Waveforms of gating signal v_{gs1} , input voltage V_{in} and output voltage V_o at full load.

On the other hand, it reveals from Fig. 6 that the experimental result of $V_{CB} = 223$ V at full load. Moreover, it is seen from the Fig. 7 that the current i_{Lo} does not start to rise immediately as the switch S_1 turns on. When the inductor current i_{Lb} rises to i_{Lo}^{min} , the diode D_2 thus becomes reverse-biased and the currents i_{Lb} and i_{Lo} increase with the same slope. Since the switch S_1 turns off, the currents i_{Lb} and i_{Lo} begin to drop with different slope. The current i_{Lb} will fall to zero in one switching period.

Fig. 6. Waveforms of gating signal v_{gs1} , input voltage V_{in} and capacitor voltage V_{CB} at full load.

Fig. 7. Waveforms of gating signal and drain-to-source voltage of switch S_2 at full load.

3.2 Soft-switching performance

Figs. 8-9 show the experimental results of gating signals and drain-to-source voltages of all the switches. It reveals that the switches are turned on after their drain-to-source voltages drop to zero. As a result, all the switches of the proposed converter are achieved ZVS operation at turn-on transition. Moreover, we also can find that the maximum voltages across switches S_1 and S_2 are nearly input voltage $V_{in} = 400$ V.

3.3 Power efficiency measurement

Figure 10 shows the measured efficiency versus various output power. The efficiency at different load conditions is also listed in the Table 2. The highest efficiency of the proposed converter is about 89.8 %. The efficiency 82.4 % of the proposed converter at full load of 400 W can be further improved by using synchronous rectification.

Table 2. Measured efficiency at various output power.

Output power (W)	100	150	200	250	300	350	400
Efficiency(%)	86.7	88.6	89.5	89.8	89.1	86.7	82.4

Fig. 8. Waveforms of gating signal v_{gs1} and drain-to-source voltage v_{ds1} of switch S_1 at full load.

Fig. 9. Waveforms of gating signal v_{gs2} and drain-to-source voltage v_{ds2} of switch S_2 at full load.

Fig. 10. Measured efficiency versus various output power.

4. Conclusions

An asymmetrical half-bridge high step-down dc-dc converter is proposed to achieve high step-down voltage conversion and ZVS operation under turn-on transition for all switches. The voltage stress across the two main switches is the input voltage $V_{in} = 400$ V. It means that the switches do not have the problem of high voltage stress. Furthermore, the experimental results of a prototype with 400V input and 48 V/400 W output thereby are presented to validate the theoretical analysis and ZVS performance of the proposed converter. The measured maximum power

efficiency of the proposed converter is 89.8 % at output power of 250 W.

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