Interleaved High Voltage Gain DC/DC Converter with Diode-Capacitor Multiplier and Coupled Inductors

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Abstract

A novel interleaved high voltage gain converter with diode-capacitor multiplier and coupled inductors is proposed to satisfy the high voltage gain, high power, and high efficiency requirements. In the proposed converter, the input-parallel configuration is used to share the input current and to reduce the conduction losses, while the diode-capacitor multiplier and coupled-inductor based voltage multiplier are employed to obtain the high voltage gain without operating at extreme duty cycle. The voltage stress of the power switches is greatly lower than the output voltage such that the low-voltage-rated MOSFETs can be employed to reduce the conduction losses and cost. Meanwhile, the diode reverse problem is alleviated by the leakage inductance of the coupled inductors. All these features make the proposed converter suitable for the high voltage gain and high power applications. Finally, a 500 W prototype with 36-400 V conversion is built and tested to demonstrate the effectiveness of the proposed converter.

Keywords: interleaved high voltage gain converter, coupled inductors, diode-capacitor multiplier.

1. Introduction

Due to the global warming problem and the fast exhaustion of the fossil fuel, much effort has been made to explore the renewable energy sources, such as the photovoltaic (PV), the fuel cells and the wind power⁽¹⁻²⁾. The renewable energy grid-connected system with PV and fuel cells calls for high voltage-gain and high-efficiency dc-dc converters because the low voltage generated by the PV and fuel cells should be boosted to a high voltage for the grid-connected system. If the line voltage is 220 Vac, a 380-400 V dc bus voltage is required for the grid-connected

inverter. However, the output voltages of PV and fuel cells are generally ranged from 24 to 40 V⁽³⁾ due to the safety and reliability considerations in the house-hold applications. Thus, a dc-dc converter with a high voltage gain is needed to boost the outputs of PV and fuel cells.

In general, a conventional boost converter can be used to provide a high voltage gain with an extreme duty cycle. However, it results in large current ripple, high switching losses, severe output diode reverse-recovery problem, and electromagnetic interference (EMI) problem⁽⁴⁾. Moreover, the voltage stresses of the power switch and the output diode are equal to the output voltage, the high-voltage-rated MOSFETs with large conduction resistor are necessary in the high output-voltage conversion system, which leads to large conduction losses and switching losses. These problems are the main limitations for the conventional boost converter. Commonly, the interleaved structure is applied in high current applications to minimize the current ripple, reduce the size of the filter components and increase the power level due to its advantages of current ripple cancellation and current-sharing performance.

In order to obtain high step-up voltage gain and high efficiency, many converter topologies have been proposed in the literature⁽⁵⁻¹³⁾. Among these achievements, they can be classified into the following categories: high step-up converters with coupled inductor⁽⁵⁻⁷⁾, high step-up converters with switched capacitor⁽⁸⁻⁹⁾, high step-up converters with voltage lift technique⁽¹⁰⁻¹¹⁾, and high step-up converters with soft-switching technique⁽¹²⁻¹³⁾. The coupled inductor serves as a transformer that is used to enlarge the voltage gain by a proper turns ratio design. The switched capacitor can be regarded as another voltage source to extend the high voltage gain conversion. As a result, the high voltage gain is achieved without operating at extreme duty cycle to alleviate the aforementioned limitation.

Fig. 1. Circuit scheme of the proposed converter.

Fig. 2. Equivalent Circuit of the proposed converter.

2. Topology and Operational Principle

The proposed interleaved high voltage gain converter is shown in Fig.1. The voltage multiplier module is composed of the second windings of the coupled inductors, two diodes and two capacitors, which is stacked on the output of the conventional interleaved boost converter. Furthermore, the diode-capacitor multiplier is inserted between the switches and output diode to extend the output voltage. There are two coupled inductors in the proposed converter. Each coupled inductor is modeled as a combination of an ideal transformer with a turns ratio n , a magnetizing inductance and leakage inductance. The coupling references of the inductors are denoted by the marks “*” and “•” as given in Fig. 1.

The equivalent circuit of the proposed converter is demonstrated in Fig. 2, where L_{m1} and L_{m2} are the magnetizing inductances, L_{k1} and L_{k2} are the leakage inductances, n is defined as the turns ratio N_s/N_p , S_1 and S_2 are the power switches, C_a and C_b are the

Fig. 3. Key waveforms of the proposed converter.

voltage-lift capacitors, C_1 , C_2 , and C_3 are the output capacitors. The key steady waveforms are shown in Fig. 3 when the converter is operated in continuous conduction mode (CCM). The duty cycle of the power switches are interleaved with 180° phase shift, and the duty cycles are greater than 0.5. There are eight operational stages in one switching period. The corresponding equivalent circuits for each stage are shown in Fig. 4.

Stage 1 [$t_0 - t_1$]: During this stage, the power switches S_1 and S_2 are in the turn-on state. All of the diodes are reverse-biased. The magnetizing inductances L_{m1} and L_{m2} as well as leakage inductances L_{k1} and L_{k2} are linearly charged by the input voltage V_{in} . This stage ends at the instant t_1 , when the switch S_2 is turned OFF.

Stage 2 [$t_1 - t_2$]: At $t = t_1$, the switch S_2 is turned OFF, which makes the diodes D_a , D_1 , and D_3 turned ON. The energy that magnetizing inductance L_{m2} has stored is transferred to the secondary side of coupled inductors charging the capacitor C_3 by the diode D_3 , meanwhile the leakage inductor current i_{Lk2} flowing through C_a and C_b , so that C_a is charged and C_b is discharged. i_{Lk2} decreases to alleviate the diode reverse recovery problem for D_a and D_1 . The voltage stress on S_2 is clamped by C_a which is equal to the output voltage of the conventional boost converter. V_{in} , L_{m2} , L_{k2} and C_b release energy to the output side. The capacitor C_b

Fig. 4. Operational stages of proposed converter.

serves as voltage source to extend the voltage gain and to reduce the switch voltage stress. This stage ends at t_2 , when the switch S_2 is turned ON.

Stage 3 [$t_2 \sim t_3$]: At $t = t_2$, the switch S_2 is turned ON. The leakage inductor current i_{lk2} increases with high rate. The current falling rate through the diode D_3 is controlled by the leakage inductance L_{k2} . This stage ends when the current flowing through the diode D_3 decreases to zero at $t = t_3$.

Stage 4 [$t_3 \sim t_4$]: At $t = t_3$, the diode D_3 is turned OFF. The operation of this stage is similar to stage 1. This stage ends when the switch S_1 is turned OFF.

Stage 5 [$t_4 \sim t_5$]: At $t = t_4$, the switch S_1 is turned OFF, which makes the diodes C_b and D_2 turned ON. The energy stored in the magnetizing inductance L_{m1} begins to transfer to the secondary side of coupled inductors charging the capacitor C_2 by the diode D_2 . Meanwhile i_{lk1} flowing through C_a and C_b , so that C_a is discharged and C_b is charged.

Stage 6 [$t_5 \sim t_6$]: At $t = t_5$, the switch S_1 is turned ON. The current falling rate through the diode D_2 is

controlled by the leakage inductance L_{k1} . When the current through D_2 decreases to zero and D_2 is turned OFF, a new switching period begins.

3. Converter Performance Analysis

To simplify the circuit performance analysis of the proposed converter in CCM, some assumptions are made as follows.

1. All of the power devices are ideal, i.e., the on-state resistance $R_{ds(on)}$ is neglected, and the forward voltage drop of the diode is ignored.
2. The capacitors are sufficiently large, such that the voltages across them can be considered as constant in one switching period.
3. The converter is under steady state and is operating in CCM with duty cycle being greater than 0.5 for high voltage gain voltage purpose.
4. Two coupled inductors are considered to be identical, namely $N_{s1}/N_{p1} = N_{s2}/N_{p2} = n$, $L_{m1} = L_{m2} = L_m$, $L_{k1} = L_{k2} = L_k$, and the coupling-coefficient $k = L_{m1}/(L_{m1} + L_{k1}) = L_{m2}/(L_{m2} + L_{k2})$.

Table 1. Magnetizing inductor voltages in the stages.

Stages Voltage	1	2	4	5
V_{Lm1}	kV_{in}	kV_{in}	kV_{in}	$k(V_{in} + V_{Ca} - V_{Cb})$
V_{Lm2}	kV_{in}	$k(V_{in} - V_{Ca})$ or $k(V_{in} + V_{Cb} - V_{C1})$	kV_{in}	kV_{in}

3.1 Voltage Gain Expression

Since the time durations of stages 3 and 6 are transition period and significantly short, only stages 1, 2, 4, and 5 are considered for the steady-state analysis. The magnetizing inductor voltages V_{Lm1} and V_{Lm2} in these stages are list in the Table 1. The time durations of stages 1, 2, 4, 5 are $(2D-1)T/2$, $(1-D)T$, $(2D-1)T/2$, and $(1-D)T$. The volt-second balance principle on L_{m1} and L_{m2} can be expressed respectively as

$$\int_0^{\frac{(2D-1)T}{2}} v_{Lm1}^{(1)} dt + \int_0^{(1-D)T} v_{Lm1}^{(2)} dt + \int_0^{\frac{(2D-1)T}{2}} v_{Lm1}^{(4)} dt + \int_0^{(1-D)T} v_{Lm1}^{(5)} dt = 0 \quad (1)$$

$$\int_0^{\frac{(2D-1)T}{2}} v_{Lm2}^{(1)} dt + \int_0^{(1-D)T} v_{Lm2}^{(2)} dt + \int_0^{\frac{(2D-1)T}{2}} v_{Lm2}^{(4)} dt + \int_0^{(1-D)T} v_{Lm2}^{(5)} dt = 0 \quad (2)$$

where T is the switching period. Substituting the parameters in Table 1 into Eq. (1) and Eq. (2), the voltage on the capacitors C_a and C_b can be given by

$$V_{Ca} = \frac{1}{1-D} V_{in} \quad (3)$$

$$V_{Cb} = \frac{2}{1-D} V_{in} \quad (4)$$

At stage 2, we have

$$V_{in} - V_{Ca} = V_{in} + V_{Cb} - V_{C1} \quad (5)$$

$$V_{C3} = V_{Ns1} - V_{Ns2} = nkV_{in} - nk(V_{in} - V_{Ca}) \quad (6)$$

Substituting Eq. (3) and Eq. (4) into Eq. (5) and Eq. (6) the voltage on the capacitors C_1 and C_3 can be expressed as

$$V_{C1} = \frac{3}{1-D} V_{in} \quad (7)$$

$$V_{C3} = \frac{nk}{1-D} V_{in} \quad (8)$$

Similarly at stage 5, the voltage V_{C2} can be derived by

$$V_{C2} = -V_{Ns1} + V_{Ns2} = \frac{nk}{1-D} V_{in} \quad (9)$$

Finally, the output voltage can be obtained by

$$V_o = V_{C1} + V_{C2} + V_{C3} = \frac{2nk+3}{1-D} V_{in} \quad (10)$$

Fig.5 shows the variation of the voltage gain versus the

Fig. 5. Voltage gain curve versus duty cycle with various k .

Fig. 6. Voltage gain curve versus turns ratio and duty cycle.

Fig. 7. Voltage gain curve comparison.

duty cycle with different coupling coefficients of the coupled inductor when the turns ratio $n=1$. It can be seen that the coupling coefficient k has only minor influence on the voltage gain. When k equals 1, the ideal voltage gain is obtained by

$$\frac{V_o}{V_{in}} = \frac{2n+3}{1-D} \quad (11)$$

Equation (11) shows that the proposed converter achieves a high voltage gain by using the diode-capacitor

multiplier and increasing the turns ratio of the coupled inductor. The ideal voltage gain versus the duty cycle of under various turns ratio of the coupled inductor is shown in Fig. 6. The ideal voltage gain versus duty cycle of the proposed converter, and the converter proposed in ⁽¹⁴⁻¹⁵⁾ with $k=1$ and $n=1$ are depicted in Fig. 7. It can be seen that the proposed converter has higher transfer gain in comparison with other converters.

3.2 Voltage stresses of switching devices

Based on the description of the operational principle, the voltage stresses on the power switches S_1, S_2 and diodes D_1, D_2, D_3, D_a , and D_b are expressed as

$$V_{S1}=V_{S2}=\frac{1}{1-D}V_{in}=\frac{1}{2n+3}V_o \quad (12)$$

$$V_{D1}=\frac{1}{1-D}V_{in}=\frac{1}{2n+3}V_o \quad (13)$$

$$V_{D2}=V_{D3}=\frac{2nk}{1-D}V_{in}=\frac{2nk}{2n+3}V_o \quad (14)$$

The switch voltage stress is much lower than the output voltage. As the turns ratio increases, the switch voltage stress decreases. As a result, the low-voltage-rated MOSFETs with low $R_{ds(on)}$ can be employed in high voltage applications. The conduction losses and cost are reduced compared with the conventional boost converter.

3.3 Limitation of the turns ratio

From the steady-state analysis, it is assumed that the duty cycle is greater than 0.5. Based on the voltage gain expression in Eq. (11), it can be concluded that the limitation of the turns ratio can be expressed as

$$n < \frac{V_o}{4V_{in}} - \frac{3}{2} \quad (15)$$

3.4 Performance Comparison

The performance comparison among the conventional interleaved boost converter, the converter published in ⁽¹⁶⁾ and the proposed converter is shown in Table 2. It can be seen that the voltage gain of the proposed converter is higher than the other converters. Clearly, the proposed converter is more suitable for high voltage gain and high output voltage applications. In the comparison of the switch voltage stress among them, the switch voltage stress of the proposed converter is much lower than the other converters. Consequently, the low-voltage-rate MOSFETs with low $R_{ds(on)}$ can be employed to reduce the conduction losses and cost compared with the other converters.

Table 2. Converter performance comparison.

Topology	Conventional interleaved boost converter	Converter introduced in [16]	Proposed converter
Voltage gain	$\frac{1}{1-D}$	$\frac{2(n+1)}{1-D}$	$\frac{2n+3}{1-D}$
Switch voltage stress	V_o	$\frac{V_o}{2(n+1)}$	$\frac{V_o}{2n+3}$
Output diode voltage stress	V_o	$\frac{(2n+1)V_o}{2(n+1)}$	$\frac{V_o}{2n+3}$
Current ripple	Large	Small	Small
Switching losses	Large	Small	Small
Reverse-recovery losses	Large	Small	Small
Conduction losses	Large	Small	Small

4. Experimental Results

In order to verify the effectiveness of the proposed converter, a 500 W prototype converter with $V_{in}=36$ V and $V_o=400$ V is built and tested. The parameters of the proposed converter are given as follows:

$$f_s = 40 \text{ kHz} ; \quad n = N_s / N_p = 1 ; \quad L_m = 160 \mu\text{H} ; \\ L_k = 1.8 \mu\text{H} ; C_1 = C_2 = C_3 = 220 \mu\text{F} ; C_a = C_b = 22 \mu\text{F} ; \\ D_1, D_2, D_3, D_a, D_b : \text{SF1606} ; S_1 \text{ and } S_2 : \text{IRFP4229}$$

The experiment results of the gate signals and drain-source voltages at $P_o=500$ W are shown in Fig. 8. The extreme duty cycle existed in the conventional interleaved boost converter is avoided because the voltage gain of the proposed converter is extended. The switch voltage stress is about 80 V with the turns ratio $n=1$. That is only one-fifth of the output voltage.

Fig. 9 shows the input current i_{in} and the currents i_{Lk1} and i_{Lk2} of the primary side of the coupled inductors at $P_o=500$ W. The peak-to-peak ripple current of i_{in} is about 1.2 A, which is much lower than those of i_{Lk1} and i_{Lk2} . The interleaved operation is helpful to reduce the input ripple current.

Fig. 10 shows the output voltage and voltages on the output capacitors C_1, C_2 and C_3 . V_o is 400 V. V_{C1}, V_{C2} , and V_{C3} are about 240 V, 80 V and 80 V, respectively. The results coincide with the expressions in Eqs. (7)-(9).

Fig. 11 shows the measured efficiency. The maximum efficiency is 97.2% at $P_o=150$ W. The efficiency at full load is appropriately 91%. The efficiency is higher than that of the conventional interleaved boost converter.

Fig. 8. Measured waveforms of v_{gs1} , v_{gs2} , v_{ds1} and v_{ds2} .

Fig. 9. Measured waveforms of i_{in} , i_{Lk1} and i_{Lk2} .

Fig. 10. Measured waveforms of V_o , V_{C1} , V_{C2} and V_{C3} .

Fig. 11. Measured efficiency versus the output power.

5. Conclusions

This paper presents an interleaved high voltage gain DC-DC converter with the diode-capacitor multiplier and coupled inductors. The voltage gain conversion ratio is enlarged and the extreme duty cycle can be avoided in the high voltage gain applications. The voltage stresses of the power switches are much lower than the output voltage. As a result, lower-voltage-rate power devices can be adopted to reduce the conduction losses. The input ripple current is decreased due to the interleaved operations. The diode-capacitor multiplier is employed to recycle the leakage energy, and absorb the turn-off voltage spikes. The output diode reverse-recovery problem is alleviated by the leakage inductances of the coupled inductors. This paper also describes the operational principle and the converter performance analysis in detail. Finally, a 500 W prototype is implemented and the experimental results are given to validate the performance of the proposed converter.

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