Low power Adaptive Viterbi Decoder with Section Error Identification

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Abstract

As mobile communication devices have evolved rapidly in our daily life, the power consumption becomes a very important issue. The channel decoders of mobile devices play a key role in transmitting information over the noisy wireless channel. Viterbi is one of the most popular error correcting channel decoders in many wireless communication devices. However, the Viterbi decoder also consumes a lot of power of portable and wireless devices, especially the Survivor Memory Unit (SMU) of decoder. In this paper, a low power adaptive Viterbi decoder with section error identification method is proposed to reduce the dynamical power consumption in varying channel noisy. We use error detecting method to identify whether the segment of the received codeword sequence is erroneous. We can disable Viterbi decoder with clock gating technique to save power consumption when finding a correct data section by error detecting method. The SMU has been split into several segments based on the truncation length of SMU for low power purpose. Subsequently, each segment of SMU can be disabled dynamically according to the instant status of error-detecting in noisy channel environment. Furthermore, we also shorten the truncation length of SMU using Path Metric Comparison Unit (PMCU) to select the optimal decoding results for achieving more dynamical power saving. With the techniques mentioned above, experimental results show that the proposed method has more than 20% power saving compared with the traditional Viterbi decoder.

Keywords: Viterbi decoder, low power, error-detection.

1. Introduction

Convolutional codes, which are forward error correction codes, have been widely deployed in many wireless communication systems to improve the limited

capacity of noisy transmission channels. Viterbi decoder⁽¹⁾ is widely used in many wireless and mobile communication systems for decoding of convolutional codes. As the mobile devices growing up rapidly, the low power design technique becomes more important for extending the battery life significantly when the devices consume lots of power. Therefore, the low power design of Viterbi decoder for wireless portable devices is valued because these devices can stand by longer if Viterbi decoder consumes less power.

The Viterbi algorithm proposed by Andrew James Viterbi in 1967 is the most popular algorithm for correcting the errors in received information affected by the channel noise when transmitting information over the communication channel. The Viterbi decoder, which is implemented according to Viterbi algorithm, performs maximum-likelihood for decoding the convolutional codes. It is in the sense that it selects the sequence which makes the received codeword most likely and uses the trellis diagram to compute the accumulated distances (Path Metrics) between the received codeword sequences and the possible transmitted sequences. The decision bits of survivor path are chosen for each correct path in the trellis and are stored in the SMU for every decoding process. After a sequence of decoding operations, the decoding data can be obtained with the closest distances compared with the original correct transmitted data.

In the early years, the area and speed of Viterbi decoder are the most important concerns in VLSI design. However, the power consumption issue of Viterbi decoder design has become a key point in the recent years. Several researches about the low power design of Viterbi decoder have been discussed to achieve power reduction. The reduced-state sequence decoding (RSSD)⁽²⁾, the M-algorithm⁽³⁾, and the T-algorithm^(4,5) have been proposed to prune significant portions of the survivors at each trellis stage that are least likely paths for reducing power consumption while executing a sequence of decisions. The processing time is

varying and depending on the number of states in the trellis. However, the algorithms still require a long time searching process based on the likelihood or metric value of the paths to find the best survivors in each trellis stage of Add-Compare-Select (ACS) loop. The extra comparison operation will affect the clock speed of the entire design and the critical path introduced by the searching processes. The pre-computation method⁽⁶⁾ was proposed to shorten the critical path introduced by the T-algorithm. The extra area and computation overheads in this field of researches need to be concerned, and the complexity and efficiency of design will be increased.

The Scarce State Transition (SST) of Viterbi decoder^(7,8) was developed to minimize the switching activities of decoded bits prior to Viterbi decoder. Using the SST Viterbi decoder, the decoded codeword sequence is likely to pass through the zero state if the condition of signal-to-noise ratio (SNR) is large enough. This technique decreases the switching activities of the internal operations in the Viterbi decoder, thus reducing the power consumption. The SST technique can result in significant reduction of dynamic power consumption. An approach which integrates the T-algorithm with the SST technique was proposed⁽⁹⁾ to reduce the ACS computation. The reconfigurable systolic Viterbi decoder⁽¹⁰⁾ has been proposed to change the truncation length according to the channel condition, resulting in reduction of power consumption. But the bit error rate (BER) is sacrificed in some condition. The SST technique and variable truncation length has also been combined with the path merging property⁽¹¹⁾ to reduce the power consumption.

A new class of convolutional codes named as the state transparent convolutional (STC) code⁽¹²⁾ has been proposed by Sarrafzadeh. The STC has the properties of pre-decoding error detection and error locating. Hence, the STC decoder can only be applied to the erroneous portion of the received sequence. It can also reduce the operation of Viterbi decoder when receiving a correct sequence. This is a very important publication for the development of low power convolutional code decoder. Based on the STC definition, the authors^(13,14) proposed some hardware implementations and tried to save the power consumption when no errors have been detected.

This paper contains five sections. Section 2 gives the overview of Viterbi decoder and the description of STC concepts. Section 3 explains the methods of proposed low power adaptive decoder. Finally, we show the experimental results in Section 4 followed by a conclusion in Section 5.

Fig. 1. The functional diagram of a Viterbi decoder.

2. Background

2.1 Traditional Viterbi decoder

A Viterbi decoder uses the traditional Viterbi algorithm, for decoding a series of codeword segments that have been encoded using the convolutional code. The typical Viterbi decoder is composed of four basic functional blocks, which are Branch Metric Unit (BMU), Add-Compare-Select Unit (ACSU), Path Metric Unit (PMU), and SMU. The architecture of Viterbi decoder is illustrated in Fig. 1.

The BMU first receives the codeword sequences and calculates the corresponding branch metrics (BMs) between the received sequences and the codewords on branches. Then, the BMs are fed into the ACSU which computes the path metrics (PMs) recursively and generates the decision bits for each state transition. Finally, the PMs of each trellis stage are stored in the PMU and the decision bits made by the ACSU are stored in SMU.

2.2 State transparent convolutional code and error detection method

The STC code⁽¹²⁻¹⁴⁾ discussed can find out the erroneous segment of the received sequence prior to Viterbi decoder. As a result, Viterbi decoder can only process these erroneous segments, and a simple method can be adopted to decode the non-erroneous segment for low power purpose. The STC is introduced as follows.

The concepts of STC are very similar to the traditional convolutional code. In the traditional convolutional code, we just take the state transition pairs of single-stage trellis into account. Fig. 2 shows the trellis diagram of traditional convolutional code. Every state has two paths to the next two states, and cannot reach other states in the next time step. However, every state in the STC code must have a path to each state for $(2, 1, K)$ code. Therefore, it sometimes has to merge several time steps into single-stage transparent pairs as shown in Fig. 3. The author⁽¹²⁾ also describes that the fully connected single-stage transparent trellis exists in $(2, 1, K)$, so the state transition pairs can be merged according to this property.

Fig. 2. 4-state trellis diagram of convolutional code

Fig. 3. 4-state trellis diagram of STC code

Based on the full connective property in $(2, 1, K)$ code, the algorithm⁽¹²⁻¹⁴⁾ can examine the possible error codeword segment. First, the received codeword sequence is split into smaller codeword segments. On the basis of the error detection method, each code segment can be represented as a unique path in the single-stage transparent trellis with initial and final states, denoted as $IS(CS_i)$ and $FS(CS_i)$ respectively, where CS_i is the codeword segment i . If the codeword segment is correct, the following relations must be satisfied simultaneously.

$$FS(CS_{i-1}) = IS(CS_i) \quad (1)$$

$$FS(CS_i) = IS(CS_{i+1}) \quad (2)$$

where CS_{i-1} , CS_i , and CS_{i+1} are the previous, current, and next codeword segments, respectively. If any of (1) and (2) is not satisfied, the current codeword segment and the corresponding codeword segment of the equation which is not satisfied are judged as erroneous segments of received

Fig. 4. The architecture of SMU

Fig. 5. The architecture of proposed low power adaptive Viterbi decoder

sequence. When the erroneous segment of the received sequence is detected, an error correction algorithm (e.g. the Viterbi algorithm) is applied to these erroneous segments. Otherwise, the simple decoder can be used to decode it instead of the channel decoder for power saving purpose.

3. The Proposed Viterbi Decoder

First of all, we use about half of the truncation length of SMU to reduce power consumption when decoding the codeword sequence in Viterbi decoder. For example, the truncation length is 48 in the rate-1/2 and $K=7$ convolutional code, we use only half of the truncation length, i.e. 24, and partition the half part of SMU into 4 segments (length 6 for each segment) as shown in Fig 4. In order to have better BER, we get the minimum PMs for the shorter truncation length instead of the convergence property for longer truncation length to pick up the optimal survivor path. Based on the STC error detection method, the erroneous segments in the codeword sequence can be detected. Then, we can easily know the condition of error occurrence and the approximate SNR in time. According to different SNR, we modify the truncation length of SMU to reduce the power consumption of Viterbi decoder. For high SNR, decoding is performed with a short truncation length to decrease the operations in SMU. We can obtain the same decoding performance and reduce the power consumption of decoder by this method. The segments 1 to 4 of SMU can be disabled respectively if there is no erroneous

Fig. 6. Flowchart of proposed low power adaptive Viterbi decoder

segment. Otherwise, the segments 1 to 4 of SMU will act regarding to each erroneous segment to get better decoding results with higher decoding performance. The architecture of proposed low power adaptive Viterbi decoder is shown in Fig 5. The algorithm of our proposed decoding method will be discussed in the following paragraph with (2, 1, 6) convolutional code as an example.

In the proposed method, three operating modes are adopted for scaling the truncation length of SMU. The truncation lengths are 0 (Mode 1), 6 (Mode 2), 12, 18, and 24 (Mode 3), respectively. The segment 2 to 3 of SMU in Mode 3 will be enabled according to the length of continuous noise occurrence. The truncation lengths are determined by comprehensive experiments for achieving the same correcting performance as the traditional Viterbi decoder. Fig. 6 illustrates the flowchart of our proposed low power adaptive Viterbi decoder with three operating modes. When receiving a codeword sequence, it will be split into codeword segments CS_{i-1} , CS_i , and CS_{i+1} . Then, equations (1) and (2) are applied to determine whether the codeword segment CS_i is erroneous due to channel noise. If not, it is

decoded with a simple decoder^(13,14) and the clock of Viterbi decoder is disabled by clock gating technique (Mode 1) to reduce the dynamic power of Viterbi decoder. Otherwise, it goes to Mode 2 and enables the first segment of SMU in the Viterbi decoder to decode the codeword segment CS_i . In Mode 2, the codeword segment CS_i is the first erroneous segment encountered, so we just enable the first segment of SMU and gate the clock signals of segments 2 to 4 of SMU for power saving purpose. After Viterbi decoder completes the operation of Mode 2, the next codeword sequence is received and split into codeword segments CS_{i-1} , CS_i , and CS_{i+1} . When enabling the Viterbi decoder in Mode 2, we can get the state of minimum PMs in PMU, the state is exactly the decoded results of previous segment CS_{i-1} due to the convergence property in Viterbi algorithm. This information in the state of minimum PMs produced by PMCU is really worthy of examination. We adapt the criterion in Mode 3 to compare the state between the minimum PMs of previous codeword segment CS_{i-1} and the initial state of current codeword segment CS_i . Therefore, the codeword segment can be detected to determine whether the segment CS_i is erroneous. If the state of minimum PMs is not equal to the $IS(CS_i)$, we treat the codeword segment CS_i in noisy condition and it has to be decoded with the segments 1 to 4 of SMU in Viterbi decoder according to the condition of SNR environment. Otherwise, we disable the Viterbi decoder and go back to Mode 1 with simple decoder to save dynamic power if there is no error encountered after Mode 3. Therefore, we can provide an efficient method to adjust the truncation length dynamically according to the varying noise condition of transmission channels for better power-saving efficiency.

4. Experimental Results

As mentioned above, the proposed low power adaptive Viterbi decoder provides three operating modes for adjusting the truncation length of SMU to reduce the operations and power consumption of SMU in Viterbi decoder. The proposed Viterbi decoder has been implemented and verified in Verilog HDL. It was also synthesized by Synopsys Design Compiler with TSMC 0.13 μm CMOS standard cell technology library. Synopsys Primetime was applied to estimate the static timing analysis and the power consumption of our proposed design with 50,000 bits of input patterns. Experimental results of power consumption with varying SNR from 1dB to 8dB are listed in Table 1, which shows that the proposed design can obtain

over 20% power saving in low SNR and about 40% in high SNR.

Table 1. Power consumption of proposed design

SNR	Power consumption (mW)	
	Conventional Viterbi decoder	Proposed Viterbi decoder
1dB	34.99 (100%)	27.60 (78.80%)
2dB	34.87 (100%)	26.00 (74.50%)
3dB	34.99 (100%)	24.00 (68.50%)
4dB	34.97 (100%)	22.50 (64.34%)
5dB	34.94 (100%)	21.00 (60.10%)
6dB	34.84 (100%)	20.47 (58.75%)
7dB	34.74 (100%)	19.94 (57.40%)
8dB	34.64 (100%)	19.40 (56.00%)

5. Conclusions

A low power adaptive Viterbi decoder which combines the concept of STC code and the idea of adjusting the truncation length of SMU has been proposed. Based on the detecting technique, our decoder uses only half of the truncation length of SMU, and provides three operating modes for scaling the truncation length of the half part of SMU. Each segment of SMU can be disabled respectively with clock gating technique according to the condition of SNR and the operating modes can be switched dynamically due to the varying noisy environment. As a result, the operations of SMU and the power consumption of the whole circuit can be significantly reduced. Experimental results have shown that the proposed design can achieve more than 20% of power saving compared with the traditional Viterbi decoder.

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