Transconductance-Mode Gain Controllable First Order Allpass Filter

Piya Supavarasuwat*, Montree Kumngern, Winai Jaikla

aDepartment of Telecommunications Engineering  Faculty of Engineering,  King Mongkut’s Institute of Technology Ladkrabang Bangkok 10520, Thailand
bDepartment of Engineering Education  Faculty of Industrial Education,  King Mongkut’s Institute of Technology Ladkrabang Bangkok 10520, Thailand

*Corresponding Author: piya.su@kmitl.ac.th

Abstract

New first order allpass filter (APF) in transconductance mode, constructed from 1 DDCCTA, 1 resistor and grounded capacitor, is presented. The transconductance gain and phase shift can be independently controlled. High input and high output impedances are achieved which make the circuit to be easily cascaded without additional buffers. The magnitude of output current can be electronically adjusted. The operation of the proposed filter has been verified through simulation results using 0.5um MIETEC CMOS technology which confirm the theoretical analysis.

Keywords:  Transconductance-mode, Allpass filter, Differential difference current conveyor transconductance amplifier (DDCCTA).

1. Introduction

“A first order all-pass filter or phase shifter is a very useful function blocks of many analog signal processing applications. It is frequently used in many active circuits such as, phase shifters, oscillators and high-Q band-pass filters(1). The first order all-pass filter with gain controllability is very useful for design in many analog circuits to avoid the use of external amplifiers, for examples quadrature oscillator(2) and multiphase sinusoidal oscillator (3) with non-interactive control for oscillation condition and oscillation frequency.” (4)

“The synthesis and design of analog filters using modern electronically controllable active building blocks (ABBs) provide flexibility and convenience for designer. These filters can be easily controlled by microcomputer or microcontroller. Also some filter circuits, employing active building blocks, can avoid the use of external resistors.” (5) The differential difference current conveyor transconductance amplifier (DDCCTA) was introduced (6). “This active building block (ABB) with three voltage inputs and two kinds of output current is constructed from the well-known advantages of the differential difference current conveyor (DDCC) and the operational transconductance amplifier (OTA). It provides the facility for the implementation of voltage and current mode signal processing. Moreover, it transconductance gain (gm) can be electronically tuned which is easy to use in the modern microcontroller or microprocessor based electronic systems.” (7)

In this paper, the transconductance mode first order allpass filter using DDCCTA as active element is presented. The proposed filter offers the following advantageous features. The proposed APF also exhibits high output input impedances, which is easy cascading in the transconductance-mode operation. The performances of the proposed circuit are illustrated by PSpice simulations, they show good agreement with the calculation.

2. Circuit Description

2.1 Differential difference current conveyor transconductance amplifier

Fig. 1. shows the circuit symbol of the DDCCTA. The internal construction of CMOS DDCCTA is illustrated in Fig. 2. The terminal relations of an ideal DDCCTA can be described by the following expressions:
For CMOS DDCCTA, the \( g_m \) is given as

\[
g_m = \sqrt{\mu C_{ox} \frac{W}{L} I_B}.
\]  

where \( \mu \) is the mobility of the carrier for NMOS transistors (M13 and M14 in Fig. 2), \( C_{ox} \) is the gate oxide capacitance per unit area, \( W \) and \( L \) are the channel width and channel length, respectively.

### 2.2 Proposed filter configuration

The proposed transconductance mode first order allpass filter is shown in Fig. 3.

It consists of one DDCCTA, single resistor and single grounded capacitor which is attractive to fabricate in monolithic chip. The proposed filter has voltage as input and current as output. The high input and output impedances are achieved. So, it can directly drive external load or connect to other circuit without any external buffer devices. The admittance transfer function is as follows:

\[
\frac{I_{out}}{V_{in}} = g_m \left( \frac{SCR-1}{SCR+1} \right).
\]

From Eq3, the phase response, gain response and natural frequency are written as

\[
\phi = \pi - 2 \arctan \left( \omega CR \right),
\]

\[
G(j\omega) = g_m
\]

\[
\omega_0 = \frac{1}{CR}.
\]

It is found from Eq. 4 - Eq. 6 that the gain and phase responses can be independently controlled. Also, the gain response can be electronically tuned.

### 2.3 Non-idea case

Taking into consideration the DDCCTA non-idealities, the relationship of the terminals given in Eq. 1 can be rewritten as

\[
\begin{align*}
I_{i1} &= I_{i2} = I_{i3} = 0; \\
V_i &= V_{i1} - V_{i2} + V_{i3}; \\
I_o &= I_i; \\
I_s &= g_m (V_x - V_y).
\end{align*}
\]

The phase response, gain response and natural frequency are written as

\[
\begin{align*}
\phi &= \pi - 2 \arctan \left( \omega CR \right), \\
G(j\omega) &= g_m \\
\omega_0 &= \frac{1}{CR}
\end{align*}
\]

where \( \beta_1, \beta_2 \) and \( \beta_3 \) are, respectively, the non-ideal voltage transfer gains between Y1-X, Y2-X and Y3-X terminals and \( \alpha \) is the non-ideal current transfer gain between X-Z terminals of the DDCCTA. These non-ideal gains slightly differ from unity by voltage-tracking error and current-tracking errors of the DDCCTA. Thus, the admittance transfer function of the proposed filter in Fig. 3 is rewritten as:

\[
\frac{I_{out}}{V_{in}} = g_m \left( \frac{SCR+1 - \beta_1 - \beta_3}{SCR+1} \right).
\]
\[
\phi = \pi - \tan^{-1}\left(\frac{\omega CR}{\beta_1 + \beta_1 - 1}\right) - \tan^{-1}(\omega CR), \tag{9}
\]
\[
G(j\omega) = \frac{\sqrt{\left(\frac{(\omega CR)^2 + (1 - \beta_1 - \beta_1)^2}{(\omega CR)^2 + 1}\right)}}{\omega_0 = \frac{1}{CR}}. \tag{10}
\]

3. Simulation Results

To verify the theoretical analysis, the proposed transconductance mode first order allpass filter in Fig. 3 was simulated with PSPICE simulation using CMOS schematic of DDCCTA as given in Fig. 2. The PMOS and NMOS transistors have been simulated by respectively using the parameter of a 0.5 µm MIETEC CMOS technology\(^{(8)}\). The optimal aspect ratios of PMOS and NMOS transistor are listed in Table I. The circuit was biased with ±2V and \(V_{bb} = -1\) V. The active and passive components are chosen as: \(I_B = 100\) µA, \(R = 10\) kΩ and \(C = 10\) pF. With this condition, the power consumption is about 3.71 mW. The simulated natural frequency is about 1.57 MHz. The simulated gain and phase responses of the filter are given in Fig. 4.

It can be found that the simulated gain and phase responses are slightly deviated from ideal responses due to the error terms as expressed in Eq. 9. Phase response for different value of R is shown in Fig. 5. This result confirms that the phase response can be tuned by R as shown in Eq. 4.

The time-domain response of the proposed filter is shown in Fig. 6 where a sine wave voltage of 500mVp-p amplitude and 1.5MHz is applied as the input to the filter and the output currents for different values of \(I_B\) are shown. It is seen that the output current can be electronically/ independently adjusted from its phase shift as expressed in Eq. 5. The output current in time domain for different value of R is shown in Fig. 7. In this result, the value of R is changed to 1kΩ, 3kΩ and 5kΩ and the phase of the output current is respectively shifted to 168.1°, 146.4° and 126.9°. It is found that the phase response can be tuned by R as shown in Eq. 4. The dependence of the output harmonic distortion of output current on input voltage amplitude is shown in Fig. 8. It can obtain from Fig. 8. that the THD is about 5.79 % when the input signal is increased to 500 mV (peak).

![Fig. 5. phase response for different value of R.](image)

![Fig. 4. Gain and phase response.](image)

![Fig. 6. Output current for different value of \(I_B\).](image)

![Fig. 7. output current for different value of R.](image)

<table>
<thead>
<tr>
<th>MOS Transistors</th>
<th>(W (\mu m))</th>
<th>(L (\mu m))</th>
</tr>
</thead>
<tbody>
<tr>
<td>(M_1-M_4)</td>
<td>1.8</td>
<td>0.7</td>
</tr>
<tr>
<td>(M_5-M_6)</td>
<td>20</td>
<td>0.7</td>
</tr>
<tr>
<td>(M_7-M_8)</td>
<td>20</td>
<td>0.7</td>
</tr>
<tr>
<td>(M_9-M_{10})</td>
<td>5.2</td>
<td>0.7</td>
</tr>
<tr>
<td>(M_{11}-M_{12})</td>
<td>58</td>
<td>1.0</td>
</tr>
<tr>
<td>(M_{13}-M_{14})</td>
<td>58</td>
<td>0.7</td>
</tr>
<tr>
<td>(M_{15}-M_{20})</td>
<td>5</td>
<td>0.7</td>
</tr>
</tbody>
</table>

\(\omega_0 = \frac{1}{CR}\).
4. Conclusions

An electronically tunable transconductance-mode first-order allpass filter with gain controllability has been introduced via this paper. It consists of 1 DDCCTA, 1 resistor and 1 grounded capacitor. So it is easy to fabricate in IC form to use in battery-powered or portable electronic equipments such as wireless communication devices. The PSpice simulation results were depicted, and agree well with the theoretical anticipation.

Fig. 8. Dependence of the output harmonic distortion of output current on input voltage amplitude

References