Investigation of Feasibility for FPGA based Zero Standby-power Type Sensor Node

Akira Yamawaki^{a,*}

^aKyushu Institute of Technology, 1-1 Sensui, Tobata, Kitakyushu 804-8550, Japan

*Corresponding Author: yama@ecs.kyutech.ac.jp

Abstract

To realize a more advanced IoT environment, more advanced edge computing is required. Therefore, we need to develop high-performance and low-power IoT devices. Hardware implementation of processing with a large computational load is effective for realizing low-power and high-performance IoT devices. For this reason, FPGAs that can flexibly configure any digital hardware according to various requirements have been attracting attention. FPGAs are equipped with countless flip-flops and logic circuits that can be reconfigured arbitrarily. Since these elements consume power even when they are not operating, standby power can be larger than that of embedded processors with low-power features. We are trying to realize a zero standby power FPGA-based IoT device in order to overcome the weakness of FPGA where standby power will increase. The proposed IoT device monitors events without power, and powers on as events occur. This adaptive wake-up/sleep manner would be suitable for IoT applications where events occur randomly. This paper develops a prototype and performs preliminary experiments using this prototype in order to verify the feasibility of FPGA-based IoT devices.

Keywords: Edge computing, IoT, FPGA, Standby power.

1. Introduction

In the IoT environment, various devices connected to the network generate data. The data is collected on the cloud, and the cloud builds big data. The cloud uses the big data to perform complex and advanced processing and make various decisions. However, the number of IoT devices and the sophistication of processing are increasing. As a result, it has become impossible to perform all processing on the cloud ⁽¹⁾.

Edge computing aims to realize a more advanced IoT environment by transferring advanced jobs that cannot be processed by the cloud alone to IoT devices (2). This technology is expected to realize smart cities, smart plants and factories, and infrastructure monitoring (3).

To realize more advanced IoT, it is necessary to make edge computing more advanced. Advanced edge computing requires high performance and low power IoT devices. Hardware implementation of processing with large computational load is effective for realizing power saving and high performance. FPGAs suitable for various processing hardware are focused on as components of IoT devices. FPGAs are equipped with countless flip-flops and logic circuits that can be reconfigured arbitrarily. Since these elements consume power even when they are not operating, the standby power can be larger than that of embedded processors with small power consumption.

We aim to realize IoT devices that can reduce standby power of FPGA to zero. Therefore, this paper tries to apply a zero standby power supply (4-6) to an FPGA-based sensor node. The proposed sensor node monitors events without power. Also, the power is turned on when an event occurs. The proposed sensor node is suitable for IoT applications where events occur randomly.

This paper clarifies the feasibility of an FPGA-based zero standby power sensor node through the development of a prototype and preliminary experiments. The rest of this paper is organized as follows. Section 2 outlines the FPGA-based zero standby power sensor node. Section 3 describes the prototype developed for conducting basic experiments. Section 4 presents the experimental results and discusses them. Finally, Section 5 concludes this paper.

2. FPGA based Zero Standby Power Type Sensor Node

Fig. 1 FZSN Architecture

2.1 Architecture

The FPGA based zero standby power-type sensor node, FZSN, has the same configuration as a microcontroller-based zero standby power-type sensor node, ZSSN⁽⁴⁻⁶⁾. This is because the architecture of ZSSN has high versatility. Figure 1 shows the architecture of FZSN.

Unlike ZSSN, FZSN has a processor-integrated FPGA instead of a microcontroller. In addition, a configuration ROM, which stores the data of the circuits configured in the FPGA after the power is turned on, is added.

The power source of the FZSN consists of a battery and an energy harvester. Energy harvesters are sensors that generate electromotive force when an event occurs, such as solar cells, piezoelectric elements, magnetic sensors, and

Peltier elements. The electromotive force of the energy harvester is used to turn on the N-type transistor that bridges the ground line until the FPGA circuit configuration is completed. After startup, FZSN accurately performs environmental sensing, information processing on FPGA, and wireless communication while using stable and sufficient power from the battery.

2.2 Action and Research Problem

FZSN attempts to realize a high-performance and low-power IoT device by performing information processing by digital hardware configured in FPGA. Circuit data for configuring digital hardware is stored in the configuration memory. Therefore, the FZSN needs to pay attention to the time required for the circuit configuration after startup. The conventional microcomputer-based ZSSN has never paid such attention. Therefore, whether FSZN can be realized or not can be applied to FPGAs is an important item to investigate. This section clarifies that the circuit configuration time is an important issue to be investigated while showing the operation overview of FZSN.

Fig. 2 shows an outline of the FZSN operations.

Fig. 2 (a): During standby, FZSN disconnects the ground line and does not consume power.

Fig. 2 (b): The energy harvester that receives the event

Fig. 2 FZSN Action

generates electromotive force. The electromotive force connects the ground line, and FZSN recovers.

Fig. 2 (c): While the electromotive force connects the ground line, the FZSN reads the circuit data from the configuration ROM and configures a digital circuit in the FPGA.

Fig. 2 (d): The FPGA that has completed the circuit keeps connecting the ground line in place of the energy harvester. The FPGA reads data from the sensor, processes the signal, and sends it to the wireless module. The wireless module wirelessly transmits the received processed data. After completing a series of tasks, the FZSN disconnects the ground line and transitions to a standby state with no power.

No one has yet examined whether FZSN can perform the above operations correctly. Furthermore, the longer the circuit is configured, the faster the battery will be consumed. As a result, unlike the conventional microcomputer-based ZSSNs, the battery replacement and charging may be more troublesome. The purpose of this paper is to examine them.

3. Experimental Setup

In order to conduct the study described at the end of the previous section, we have developed a prototype applying the zero standby power supply mechanism to a commercially available FPGA board. Figure 3 is a block diagram of this prototype.

The FPGA board is Digilent Cmod A7. This FPGA board is equipped with Xilinx Artix-7 FPGA. The combination of N-type and P-type transistors realizes a switch for bridging the ground line. When the ground line is cut, the FPGA pins are pulled to the power supply level. At

Fig. 3 Block Diagram of Prototype FZSN

that time, the P-type transistor is used to electrically disconnect the connection between the output pin of the FPGA and the gate of the N-type transistor.

To estimate the battery life, the current consumed by the FZSN during operation is needed. Therefore, a shunt resistor is inserted in the power supply line. The voltage applied between the shunt resistors is amplified by 25 times with the instrumentation amplifier, Maxim Integrated MAX9923T. Furthermore, the amplified voltage is amplified 46.4 times by the non-inverting amplifier using Linear Technology LT1013. The current consumption I_{exe} during operation is calculated by Eq. (1).

$$I_{exe} = V_p / 25 / 46.4 / 0.2 [A] \quad (1)$$

From this current consumption, the battery duration BL is estimated by Eq. (2) ⁽⁴⁾.

$$BL = \frac{8.38 \times BC [Ah]}{I_{exe} [A] \times T_{exe} [s] \times N} [year] \quad (2)$$

Here, T_{exe} is the execution time, and N is the number of revivals per day.

The hardware on the FPGA was a simple circuit that counted up a 32-bit counter while driving the gate of an N-type transistor for 100 ms. The operating frequency is 100MHz.

4. Experimental Result and Discussion

Figure 4 shows the waveforms observed on the prototype. The current consumption was calculated using equation (1) while observing V_p in Fig.3. The gate voltage of the N-type transistor is shown so that the operation of the prototype can be easily understood.

Figure 4 shows that the configuration time of the circuit is about 90 ms. The current consumption during that time is about 2.0 mA. After the circuit configuration, the FPGA drives the N-type transistor at the voltage level of 3.3V and operates the counter.

The processing time during that time was about 100 ms, and the current consumption was about 1.0 mA. The execution time is $90\text{ms} + 100\text{ms} = 190\text{ms}$. The average current consumption during operation is $2.0 \times 90 / 190 + 1.0 \times 100 / 190 = 1.47 \text{ mA}$.

When the measured parameters are input into equation (2) and calculated, when N is 1, the battery life is about 50,000 years. If N is 5000, the battery life will be about 10 years. For applications with less than 5000 activations per day, the FZSN can achieve a battery life of 10 years. We believe that FZSNs with a battery time of more than 10

Fig. 4 Experimental Result

years can be used in various applications.

The current consumed by the FPGA depends on the size of the circuit. A study that includes that perspective is a topic for the future.

5. Conclusions

To realize a more advanced IoT environment, it is necessary to realize more advanced edge devices. Edge devices that use FPGAs can realize high-performance and low-power edge devices by implementing high-load processing hardware. However, the FPGA needs to configure the circuit at startup. That time can further increase power consumption. Furthermore, the huge internal resources of the FPGA consume large amounts of standby power, which can adversely affect battery life.

In this study, we examined whether our proposed zero standby power mechanism can be applied to sensor nodes using FPGA. Experimental results show that a zero standby sensor node based on FPGA is feasible. In addition, the battery life was estimated including the circuit configuration time. The results show that sufficient battery life can be achieved in various applications.

Acknowledgment

This work was supported by JSPS KAKENHI Grant Number 17K00126.

References

- (1) R. K. Naha, S. Garg, D. Georgakopoulos, P. P. Jayaraman, L. Gao, Y. Xiang, and R. Ranjan: "Fog Computing: Survey of Trends, Architectures, Requirements, and Research Directions", IEEE Access, vol. 6, pp.47980-48009 (2018)
- (2) M. Fazio, R. Ranjan, M. Girolami, J. Taheri, S. Dustdar, and M. Villari: "A Note on the Convergence of IoT, Edge, and Cloud Computing in Smart Cities", IEEE Cloud Computing, Vol. 5, No. 05, pp.22-24 (2018)
- (3) B. Varghese, M. Villari, O. Rana, P. James, T. Shah, M. Fazio and R. Ranjan: "B. Varghese and M. Villari and O. Rana and P. James and T. Shah and M. Fazio and R. Ranjan", IEEE Cloud Computing, Vol. 5, No. 06, pp. 9-20 (2018)
- (4) Akira Yamawaki and Seiichi Serikawa: "Battery Life Estimation of Sensor Node with Zero Standby Power Consumption", Proceedings of 19th IEEE International Conference on Computational Science and Engineering, pp.166-172 (2016.8)
- (5) Akira Yamawaki and Seiichi Serikawa: "Door Monitoring System Using Sensor Node with Zero Standby Power", Transactions on Engineering Technologies: International MultiConference of Engineers and Computer Scientists 2016, pp.73-87 (2017.5)
- (6) Akira Yamawaki, Mayu Yamanaka and Seiichi Serikawa: "A sensor node architecture with zero standby power on wireless sensor network", Artificial Life and Robotics, vol. 20, no. 3, pp.210-216 (2015.10)