A Method for Weight Set Compaction in Power Aware Multiple Weighted Random BIST

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Abstract

This paper presents a multiple weight set weighted random BIST scheme to perform power aware test which takes into account peak power constraint and reducing the number of required weight sets. Exceeding the peak power budget during test provokes problems such as erroneous circuit function due to IR drop and electrical damage to the circuit. However, excessive power reduction during test can degrade fault screening capability of the test since the test environment becomes substantially less stringent than the environment in which the device is actually used. Therefore, controlling power consumption during test operation is important to perform adequate testing. In this paper we address both these problem simultaneously. The main contribution of this paper is to provide an efficient scan based weighted random BIST scheme within power constrain. We assume full scan environment, test per scan testing, and single stuck-at fault model. Genetic algorithm (GA) based optimization method is proposed to find effective weight sets.

Keywords: BIST, weighted random testing, power-aware testing, scan based testing.

1. Introduction

Power consumption during scan test mode is generally much higher than the power consumed in normal operation because the scan test scheme changes circuit behavior, and the test patterns generated by automatic test pattern generators (ATPG) tend to induce high switching activity⁽¹⁾. The high power consumption during test mode can provoke many problems such as cooling difficulties of heat dissipation, circuit damage and deterioration of overall product yield. Especially in the current low power designs,

low power dissipation during test mode without any test quality degradation is becoming important, and methods have been presented to solve these problems⁽¹⁾.

As one of the efficient design for testability (DFT) solutions, built-in self test (BIST) scheme is being as a mature approach for VLSI designs that can help avoid the difficulties of external testing. The BIST circuit is embedded in a VLSI chip occupies a small chip area. Main benefit of BIST concept is that testing can be performed under high observable and high controllable environment, because there is no limitation of the number of external pins. In BIST, pseudo-random pattern testing using linear feedback shift register (LFSR) and multiple input signatures register (MISR) are usually exploited since their low impact on hardware overhead is attractive. However, it is well known that often a large number of LFSR generated test patterns are required to get acceptable fault coverage, and yet random pattern resistant (r.p.r.) faults are hard to detect despite applying huge number of test patterns. Furthermore, low correlation between any successive two random test patterns increases power consumption during BIST. Besides, excessive scan test power consumption, such as scan-shift power and capture power during scan test is also becoming a major concern⁽²⁾. Several low-power BIST approaches have been proposed to address these problems. In reference (3), weighted random test patterns which were assumed to induce high switching activity were inhibited, and LFSR reseeding method has been proposed. Scan-shift toggle suppression and test pattern suppression techniques have been proposed in reference (4). Low transition test pattern generation method has been proposed in reference (5), and a 3-weight weighted random BIST method and scan-reordering have been proposed in reference (6). Weighted random BIST scheme with special scan cell design for bit fixing has been proposed in reference (7). In our

previous study, we exploited fault clustering using circuit topology to control power consumption⁽¹⁴⁾.

This paper presents a weight set compaction method in multiple weight set weighted random BIST approach to perform power aware test which considers the constraint of peak power consumption during scan capturing. We assume full scan environment and test per scan testing. Generally, exceeding peak power consumption during test sequence induces many problems, such as erroneous circuit function due to IR drop and electrical damage to the circuits^{(1),(11)}. In many previous research works, they have been focusing on energy and power reduction to as low as possible. This can degrade fault screening capability since the test environment might become less stringent than the actual use environment. Since large number of weight set for weighted random pattern generation would increase the overhead of BIST circuit, the number of required weight sets should be reduced.

The main contribution of our approach is to provide an efficient scan based weighted random BIST scheme within peak power constraint and adequate energy consumption. The major problems of power consumption in scan testing are scan shift power violation and scan capture power violation⁽¹¹⁾⁽¹³⁾. The scan shift power can be reduced by insertion of gating logic on scan cells output, reordering scan cells, dividing a scan chain and so on^{(9),(10),(12)}. However, peak power of scan capturing on random BIST scheme is hard to manage, because it depends on consecutive two patterns. Although several approaches had been shown to control peak power consumption^{(11),(13)}, no approaches have been found for multiple weighted random testing. In this paper, we focused on avoiding peak power violation during scan capturing. A weight biasing procedure is performed to restrict the amount of test power consumption. The weights are biased toward 0 or 1 in order to adjust the amount of power consumption. Fundamental idea of this approach is that a weight set looking after larger number of faults might create higher power consumption, and a weight set focusing on small number of faults might create low power consumption. Assuming single stuck-at fault model, genetic algorithm (GA) based optimization method is proposed to find effective weight sets.

The rest of this paper is organized as follows. Section 2 describes power consumption models and concept of power reduction. Section 3 introduces architectures of proposed BIST method. Section 4 describes GA based weight set optimization method. Experimental results for a

set of benchmark circuits are presented in Section 5. Finally, conclusion is described in Section 6.

2. Concept of Power Reduction

2.1 Power Consumption Model and Estimation Metric

Power consumption in typical CMOS technology devices can be classified into static or dynamic. Dynamic power dissipation is caused by switching activity of CMOS transistors. Charging and discharging of load capacitances connecting from the transistors, and instantaneous short circuit during dynamic turning phase of the transistors are the main sources of the dynamic current flow. In recent VLSI designs, dynamic power dissipation is still dominant in standard CMOS devices because dynamic current flow is relatively larger than the static current flow⁽¹⁾.

As dynamic power consumption model, we use switching activities of gates in CMOS circuits since the switching current contributes to power consumption significantly and reflects actual power consumption well. The weighted switching activity (WSA) is exploited to provide a better estimate of the actual power consumption, which is defined as the number of transitions on a gate output signal multiplied by its capacitance⁽⁴⁾. For simplicity, we used the number of fan-outs of each gate as the amount of the load capacitance. Therefore, the total power consumption is derived from the sum of the WSA of all gates. The factors that are important for evaluating power consumption are: energy, average power, instantaneous power, and peak power. These are defined below⁽⁸⁾.

- Energy. Energy is the total switching activity during test application, and is derived as the sum of WSA applying all test patterns.
- Average power. Average power is the total distribution of power over a time period. This is derived from the ratio of the energy to the number of required test patterns. Elevation of average power increases the thermal load and might cause of structural damages.
- Instantaneous power. Instantaneous power is the value of power consumption at any given instant. This value is derived from the sum of WSA of each gate by applying consecutive two test patterns.
- Peak power. Peak power is the highest power value at any instant. We define it as the highest instantaneous power consumption during test period, so that it is

derived from the highest sum of WSA of each gate by applying consecutive two patterns during scan capturing⁽¹³⁾.

2.2 Controlling Power Consumption

Minimizing test length and reducing average power are two common ways to reduce total energy. Generally, there exists a trade-off between the two approaches^{(8),(10)}. Figure 1 shows a rough outline of the power consumption (WSA) during consecutive two test patterns. If test length is minimized without any loss of fault coverage, such as during ATPG test patterns, the average power and peak power will be increased by its high switching activities. The average power could be simply reduced by making test length longer; however, it increases the total energy consumption. Therefore, finding an efficient trade-off point between test length and average power is important to perform effective testing under the power constraints. On the other hand, excessive power reduction of test might be inappropriate for screening faults because the electrical and thermal test environment becomes relatively slack compared to the normal operation of the circuit. Thus, it is important to consider obtaining adequate average power consumption with the restriction of peak power consumption within a design budget for efficient testing.

Fig. 1. Outline of power consumption between two consecutive test patterns.

In order to control the amount of power consumption, we propose a weight biasing method. Figure 2 shows a basic outline of the relationship between power consumption and the size of target fault cluster. The fault cluster is defined as a set of target faults for test pattern generation. If the generated test patterns are able to detect many faults, higher switching activities will occur in the circuit under test (CUT). On the contrary, test patterns

generated by exploiting strongly biased weight, which target small number of faults will induce small switching activity. Therefore, the approximate amount of power consumption is able to be controlled by handling the size of fault cluster.

Fig. 2. Relationship between power consumption and fault cluster size.

3. Proposed Weighted Random BIST Scheme

We assumed full-scan and test per scan architecture in our proposed weighted random BIST scheme. For biasing LFSR generated patterns, we proposed two cases of weight variations: 9 kind of weight (0, 1, 0.5, 0.125, 0.25, 0.75 and 0.875). Figure 3 shows a proposed BIST architecture which is almost as same as conventional weighted random BIST configurations. Thus, we have not discuss about hardware overhead of the BIST circuit.

Fig. 3. Proposed Weighted Random BIST architecture.

4. Weight Sets Computation Algorithm

In order to obtain optimal weight sets for random test

pattern generation, we proposed GA based optimization method. Figure 4 shows proposed weight sets computation algorithm. First of all, whole faults excepting redundant faults are divided into two groups by applying equi-probable random patterns. The one is for r.p.r. faults and the other group is easy to detect faults. Weight sets are generated for r.p.r faults group firstly. Redundant fault are eliminated by pre-processed ATPG.

Then, GA based weight set optimization are performed. If the result of the weight set optimization could not pass the constraint of peak power consumption, the weights are biased toward 1 or 0, and optimization will be performed again (Figure 4 (1)).

In the GA based weight set optimization, ATPG test patterns are exploited to take care r.p.r. faults which can be detect only particular test patterns. The ATPG test pattern for the fault is put into the initial population of GA based procedure. This would help to achieve 100% fault efficiency.

Weight sets shifting is performed to reduce the number of weight sets (Figure 4 (2)). In this procedure, after obtaining 4 weight sets, the first weight set is excluded and the rest of 3 weight sets are evaluated by fault simulation. Then a new weight set is derived by weight set optimization procedures and the weight set is appended to the 3 weight sets. Again, the oldest weight set is excluded. This procedure repeats 16 times to get 4 efficient weight sets. After this procedure, The 4 weight sets are fixed and other weights sets are generated for still undetected faults.

Fig. 4. Flow of Weight Sets Computation Algorithm.

5. Experimental Results

Experiments were performed on a set of ITC'99

benchmark circuits. Before performing the experiments, we obtained ATPG test patterns for each benchmark circuit to eliminate redundant faults and to take care r.p.r faults in the GA based weight sets optimization. The number of backtrack limit in the ATPG was 1,000,000. ATPG aborted faults were not eliminated from target faults. Initially, we applied 131,072(=217) equi-probable random test patterns to determine the amount of the maximum peak power. The amount of target peak power is derived from multiplying “1 - reduction rate” by the maximum peak power. We assumed 0% 10% 20% 30% 40% 50% and 60% peak power reduction rates respectively. In the simulation, weight variation is 9-weight (Fix 0, Fix 1, 0.125, 0.25, 0.5, 0.75 and 0.875). Table 1 shows the result of the experiment.

In the table 1, “0% target peak power reduction rate” means that no constraint to peak power dissipation has been applied. The “fault efficiency” in the table was calculated by excepting ATPG undetectable faults, but ATPG aborted faults were included. In case of b14 circuit, aborted faults in ATPG were detected in the optimization process. The “Average Power” represents average power (WAS) of consecutive 2 random patterns. The “Peak Power” represents the maximum peak power (WSA). Almost all circuits satisfy the target peak power reduction rates with archiving high fault coverage. Since the proposed GA based optimization process focused on accomplishing target peak power constraint, average power consumptions tended to be increasing in case of slack target peak power constraints.

Table 1. Experimental results on ITC'99 benchmark circuits.

Circuit	Target Peak Power Reduction Rate (%)	# of Required Weight Sets	Fault Efficiency (%)	# of Required Vectors	Peak Power (WSA)	Peak Power Reduction Rate (%)	Average Power (WAS)	Average Power Reduction Rate (%)
b12	60	23	100.0	14944	295	37.7	146	42.9
	50	13	100.0	16096	370	47.3	174	51.2
	40	8	100.0	14816	444	56.8	225	66.2
	30	6	100.0	8352	518	66.2	236	69.4
	20	4	100.0	10400	581	74.3	308	90.6
	10	4	100.0	8096	647	82.7	369	108.5
	0	4	100.0	10816	723	92.5	398	117.1
	0	4	100.0	10816	723	92.5	398	117.1
b14	60	50	98.8	126944	4280	39.3	2173	39.4
	50	48	99.3	121984	5196	47.7	2480	45.0
	40	40	99.3	95552	6203	56.9	2733	49.6
	30	34	99.3	87904	7234	66.4	3096	56.2
	20	38	99.3	78432	8268	75.9	2886	52.3
	10	34	99.3	85920	9133	83.8	3385	61.4
	0	35	99.3	86400	10112	92.8	3435	62.3
	0	35	99.3	86400	10112	92.8	3435	62.3
b15	60	46	93.9	100288	2172	39.8	1173	43.0
	50	46	95.9	92480	2591	47.4	1394	51.1
	40	42	96.6	98464	3108	56.9	1677	61.4
	30	39	96.7	88256	3791	69.4	1948	71.4
	20	30	96.7	72064	4145	75.9	2201	80.6
	10	25	96.7	66432	4583	83.9	2145	78.6
	0	25	96.7	62688	4714	86.3	2191	80.3
	0	25	96.7	62688	4714	86.3	2191	80.3

Table 2 shows the result without using weight set compaction procedure. Table 3 shows comparison between Table1 and Table2 (Table1 – Table2) in order to show the effectiveness of weight set compaction. In almost all cases, the required number of weight set is reduced. This

will contribute to reduction of BIST circuit.

Table 2. Experimental results without using weight set compaction.

Circuit	Target Peak Power Reduction Rate (%)	# of Required Weight Set(s)	Fault Efficiency (%)	# of Required Vectors	Peak Power (WSA)	Peak Power Reduction Rate (%)	Average Power (WSA)	Average Power Reduction Rate (%)
b12	60	25	100.0	17152	295	37.7	154	45.3
	50	16	100.0	14784	370	47.3	175	51.5
	40	10	100.0	13696	444	56.8	198	58.2
	30	6	100.0	14912	512	65.5	280	82.4
	20	5	100.0	9472	588	75.2	276	81.2
	10	4	100.0	8096	647	82.7	369	108.5
	0	5	100.0	9088	682	87.2	355	104.4
b14	60	61	99.1	143328	4274	39.2	2169	39.3
	50	52	99.3	117216	5364	49.2	2480	45.0
	40	44	99.3	113248	6207	57.0	2762	50.1
	30	37	99.3	92320	7215	66.2	3026	54.9
	20	40	99.3	95520	8254	75.7	3227	58.5
	10	37	99.3	74272	9105	83.6	3473	63.0
	0	40	99.3	102752	10074	92.4	3404	61.7
b15	60	55	94.4	95200	2096	38.4	1136	41.6
	50	60	96.5	114784	2708	49.6	1386	50.8
	40	48	96.7	115936	3109	56.9	1591	58.3
	30	39	96.7	100608	3658	67.0	1847	67.7
	20	29	96.7	70368	4135	75.7	2028	74.3
	10	26	96.7	81344	4649	85.1	2498	91.5
	0	26	96.7	80320	4810	88.1	2407	88.2

Table 3. Comparison between Table1 and Table2
(Table1 – Table2).

Circuit	Target Peak Power Reduction Rate (%)	# of Required Weight Set(s)	Fault Efficiency (%)	# of Required Vectors	Peak Power (WSA)	Peak Power Reduction Rate (%)	Average Power (WSA)	Average Power Reduction Rate (%)
b12	60	-2	0.0	-2208	0	0.0	-8	-2.4
	50	-3	0.0	1312	0	0.0	-1	-0.3
	40	-2	0.0	1120	0	0.0	27	7.9
	30	0	0.0	-6560	6	0.8	-44	-12.9
	20	-1	0.0	928	-7	-0.9	32	9.4
	10	0	0.0	0	0	0.0	0	0.0
	0	-1	0.0	1728	41	5.2	43	12.6
b14	60	-11	-0.4	-16384	6	0.1	4	0.1
	50	-4	0.0	4768	-168	-1.5	0	0.0
	40	-4	0.0	-17696	-4	0.0	-29	-0.5
	30	-3	0.0	-4416	19	0.2	68	1.2
	20	-2	0.0	-17088	14	0.1	-341	-6.2
	10	-3	0.0	11648	28	0.3	-88	-1.6
	0	-5	0.0	-16352	38	0.3	31	0.6
b15	60	-9	-0.5	5088	76	1.4	37	1.4
	50	-14	-0.6	-22304	-117	-2.1	8	0.3
	40	-6	-0.1	-17472	-1	0.0	86	3.2
	30	0	0.0	-12352	133	2.4	101	3.7
	20	1	0.0	1696	10	0.2	173	6.3
	10	-1	0.0	-14912	-66	-1.2	-353	-12.9
	0	-1	0.0	-17632	-96	-1.8	-216	-7.9

6. Conclusion

This paper has proposed a multiple weight set weighted random BIST scheme with taking into account peak power constraint on scan testing and with performing weight set compaction. Experimental results showed that effective weight sets within peak scan capture power constraint could be obtained by proposed method.

References

- (1) P. Girard : "Survey of Low-Power Testing of VLSI Circuits," IEEE Design & Test of Computers, Volume 19, Issue 3 (May 2002), pp. 82-92, 2002
- (2) Xiaoqing Wen, K. Miyase., T. Suzuki, Y. Yamato, S. Kajihara, Laung-Terng Wang, and K.K Saluja : "A Highly-Guided X-Filling Method for Effective Low-Capture-Power Scan Test Generation," Int. Conf. on Computer Design 2006 (ICCD 2006), pp.251-256, 2006
- (3) P. Girard, L. Guiller C. Landrault, and S. Pravossoudovitch : "A Test Vector Inhibiting Technique for Low Energy BIST Design," 17Th IEEE VLSI Test Symposium (VTS'99), 1999
- (4) Gerstendorfer, and H.-J. Wunderlich : "Minimized Power Consumption for Scan-based BIST," Int. Test Conf. 1999 (ITC99), pp.77-84, 1999
- (5) S. Wang and S.K. Gupta : "LT-RTPG: A New Test-Per-Scan BIST TPG for Low Heat Dissipation," Int'l Test Conf. (ITC 99), pp. 85-94, 1999
- (6) S. Wang : "Generation of Low Power Dissipation and High Fault Coverage Patterns for Scan-Based BIST," Proc. of Int. Test Conf. 2002 (ITC'02), pp.834-843, 2002
- (7) S. Ghosh, E. MacDonald, S. Basu, and N. A. Touba : "Low-Power Weighted Pseudo-Random BIST Using Special Scan Cells," the 14Th ACM Great Lakes Symp. on VLSI (GLS-VLSI 2004), pp. 86-91, 2004
- (8) B. Pouya, and A. L. Crouch : "Optimization Trade-offs for Vector Volume and Test Power," Proc. of Int. Test Conf 2000 (ITC'00), pp. 873-881, 2000
- (9) N. Nicolici and X. Wen : "Embedded Tutorial on Low Power Test," ets, 12th IEEE European Test Symposium (ETS'07), pp.202-210, 2007
- (10) Synopsys white paper : "Testing Low Power Designs with Power Aware Test," <http://www.synopsys.com/>, April 2010
- (11) R. Sankaralingam and Nur A. Touba : "Controlling Peak Power During Scan Testing," 20th IEEE VLSI Test Symposium (VTS2002), pp.153-159, 2002
- (12) C. P. Ravikumar, M. Hirech and X. Wen : "Test Strategies for Low Power Devices," Design, Automation and Test in Europe, 2008 (DATE2008) pp.728-733, 2008
- (13) N. Badereddine, P. Girard, S. Pravossoudovitch, C. Landrault and A. Virazel : "Minimizing Peak Power Consumption during Scan Testing: Test Pattern Modification with X Filling Heuristics," Proc. of Design and Test of Integrated Systems in Nanoscale Technology 2006 (DTIS2006), pp.359-364, 2006
- (14) Hiroshi Yokoyama, Hideo Tamamoto and Kewal K. Saluja : "Controlling Peak Power Consumption for Scan Based Multiple Weighted Random BIST," 2010 19th IEEE Asian Test Sym .(2010), pp.147-152, 2010