Chip on chip bonding technology for fine pitch connection with Al-Si/TiN bumps

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1. Abstract

Recently, we reported COC (chip on chip) device with Au stud bumps. ⁽¹⁾ The conductivity is appropriate. However, there is not enough working space in the Au stud bumps for 3D connection. So it is not a suitable bump for fine pitch COC devices. In this report, we fabricate Al-Si/TiN bumps for fine pitch COC devices. The edges are sharp and the top surface has a high degree of flatness; it is thus suitable for fine pitch COC devices.

Keywords: Al-Si/TiN bump, chip on chip, fine pitch, SPAD

2. Introduction

A number of compact single-chip CMOS single-photon avalanche diode (SPAD) imaging arrays have been proposed for time-correlated single-photon or photon-counting applications, such as fluorescence-lifetime imaging microscopy, fluorescence correlation spectroscopy, wave front sensing in astronomy, ranging, and 3-D cameras. ⁽²⁻⁶⁾

However, the imagers typically have low fill factor, i.e. a low proportion of the pixel's surface that is light sensitive, due to in-pixel circuitry. ⁽⁷⁾

3D integration technologies have several merits in that they not only ensure low power, high speed, and high density, but also high fill factor for CMOS SPAD imaging arrays. ⁽⁸⁻¹²⁾ Recently, we fabricated and reported a COC device with Au stud bumps. ⁽¹⁾ However, the bump shapes are not appropriate for fine pitch. Fig. 1 shows a SEM cross-section view of Au stud bumps. ⁽¹⁾ The bump edges are round so that there is not enough working space, since in total ("a" and "b" space) occupies 6 μm out of 45 μm (bump size). Therefore, the working space exhibits a 13-% loss.

So we propose a 3D integration technology with Al-Si/TiN bumps to improve the fine pitch in COC devices. The edges are sharp and the top surface has a high degree of flatness; it is thus suitable for fine pitch COC devices.

Fig. 1. SEM cross-section view of Au stud bump.

3. COC devices layout

We designed 2 types of IC (bottom-side chip, top-side chip) for a COC device with Al-Si/TiN bumps. Fig. 2 shows the overlapping layout of bottom-side chip (pink color) and top-side chip (black color). The COC layout has 10 measurement circuits for testing the 3D connection resistance. There are 2 types of bump shapes (square type and rectangle type). And the bump area was varied from 480 μm^2 to 4489 μm^2 .

Fig. 3 shows the resistance measurement of the 3D connection. This circuit is a four-terminal sensing setup. It uses an electrical impedance measuring technique based on

separate pairs of current-carrying (A and B) and voltage-sensing (C and D) electrodes.

Fig. 2. Layout of bottom-side chip (pink color) and top-side chip (black color).

Fig. 3. Resistance measurement image of 3D connection.

4. Top-side and bottom-side chips

We fabricated two chips (top-side chip and bottom-side chip) at TU Delft. Fig. 4 and Fig. 5 show the top-side chip and bottom-side chip, respectively, where the black area ("a") is a SiO_2 layer. A layer of 800 nm was deposited by PECVD on c-Si substrate. The brown pattern ("b") are Al-Si/TiN layers. A 6- μm Al-Si layer was deposited on SiO_2 by sputtering for making 3D connection bumps. A 30-nm TiN layer was deposited on Al-Si by sputtering as an oxidation resistant layer.

Fig. 4. Top-side chip

Fig. 5. Bottom-side chip.

5. COC bonding

The COC device was bonded with ACP (anisotropic conductive paste). The ACP (TAP0402E) has Ni particles and epoxy resin. It supported 3D connections and adhesion between top and bottom chips. Fig. 6 shows ACP-coated bottom-side chip.

Fig. 6. ACP-coated bottom-side chip.

Fig. 7 shows COC device with Al-Si/TiN bumps. The COC device is bonded using a flip chip bonder. The bonding conditions were 10 N, 20 secs in 160 degrees. The COC device cut the red line for checking 3D connection by SEM. We checked several cross-section views.

Fig. 7. COC device with Al-Si/TiN bumps.

Fig. 8(a) shows a SEM image of the cross-section view of the COC device. Fig. 8 (b)-(d) are 3D connection point (A, B, C) views of Al-Si/TiN bumps. The Al-Si/TiN bumps still keep sharp edges and flat tops after bonding. The entire bonding area is operational. So the Al-Si/TiN bumps are appropriate for fine pitch compared with Au stud bump. The point B and C have little gap compared with point A. The gaps increase slightly, commensurately to left side.

(a)COC device

(b) Point A.

(c) Point B.

(d) Point C.

Fig. 8. SEM cross-section view.

6. 3D connection characteristics

We measured 3D connection characteristics by four-terminal sensing. Fig. 9 shows I-V characteristics of the 3D connection resistance. The connection is using Al-Si/TiN bumps. The output voltage increases linearly with the supplying current with a resistance of 0.726Ω . Fig. 10 shows the resistance of a square type electrode for each area. The resistance decreases commensurately by the connection area without 1 point. The point located on left side in Fig. 8(a). The little gap loss the connecting area on the left side. We

have to care the flat condition for reducing bonding errors. The minimum resistance is 0.2Ω at $2025 \mu\text{m}^2$. The resistance of conventional method (using Au stud bump) is 2.18Ω at $1963 \mu\text{m}^2$. So the resistance of Al-Si/TiN bumps are lower than the Au stud bumps.

Fig. 9. 3D connection using Al-Si/TiN bumps characteristics.

Fig. 10. Resistance of square type electrode for each area.

Fig. 11 plots the resistance of rectangle shaped electrodes for each area. The resistance decreases commensurately by the connection area without 2 points. These point located on left side in Fig. 8(a). The little gap also loss the connecting area on the left side.

Fig. 11. Resistance of rectangle type electrode for each area.

Conclusions

To improve the fill factor of CMOS-SPAD imaging arrays, Al-Si/TiN bumps are used on a COC device instead of Au stud bumps. The Al-Si/TiN bumps still keep sharp edges with flat tops after bonding. The entire surface of the chip was successfully bonded. So the Al-Si/TiN bumps are appropriate for fine pitch compare with Au stud bump. The 3D contact resistance was measured by four-terminal sensing. The resistance decreases commensurately by the connection area. The minimum resistance is $0.2\ \Omega$ at $2025\ \mu\text{m}^2$.

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